

Title	Page
Cover Sheet	1
Block Diagram	2
Power Deliver Chart	3
Clock Distribution	4
PWRGD&RESET Map	5
GPIO/MSIC TABLE	6
POWER ON SEQUENCE	7
FM2 PCIE I/F	8
FM2 DDR3 I/F(A)	9
FM2 DDR3 I/F(B)	10
FM2 DISPLAY/MSIC	11
FM2 POWER/GND	12
FM2 CAPS & VCORE CAP	13
DDR3 XMM1 CH-A	14
DDR3 XMM2 CH-A	15
DDR3 XMM3 CH-B	16
DDR3 XMM4 CH-B/Cap For DIMM	17
EMI Reserved	18
HUDSON ACPI/USB/AZ/GPIO	19
HUDSON PCIE/PCI/APU/LPC/CLK	20
HUNDSON SATA/VGA/HWM/SPI	21
HUDSON POWER/GND	22
HUDSON STRAPS	23
DVI1 CONN	24
DVI2 CONN.	25
LAN AR8151	26
SATA/ FAN	27
AUDIO 92HD73E	28
AUDIO CONNECTOR	29
ACPI UPI & LED	30
SUPER I/O F71808A	31
SYS POWER	32
DDR POWER	33
FCH CORE	34
USB POWER	35
USB 2.0 CONN	36
USB 3.0 CONN	37
ISL6277 3+2 Phase(A)	38
ISL6277 3+2 Phase(B)	39
PCIE X16 SLOT	40
PCIE X1 SLOTS	41
PCIE X1 mini card	42
ATX & Front Panel	43
Auto BOM manual	44
History	45



MS-7778 VER: 0A

uATX 9.6" x 9.6"

CPU:

AMD FM2

System Chipset:

AMD - Hudson D3

On Board Chipset:

Fintek Super I/O -- F71808A

LAN -- Atheros AR8161L

HD Codec -- IDT 92HD73E

BIOS -- SPI ROM 64M

Main Memory:

DDR III X 4 (Max 16GB)

Expansion Slots:

PCI Express X16 Slot * 1

PCI Express X1 Slot * 3

PCI Express X1 Slot *1 for MINI CARD

PWM:

Controller -- Intersil ISL6277



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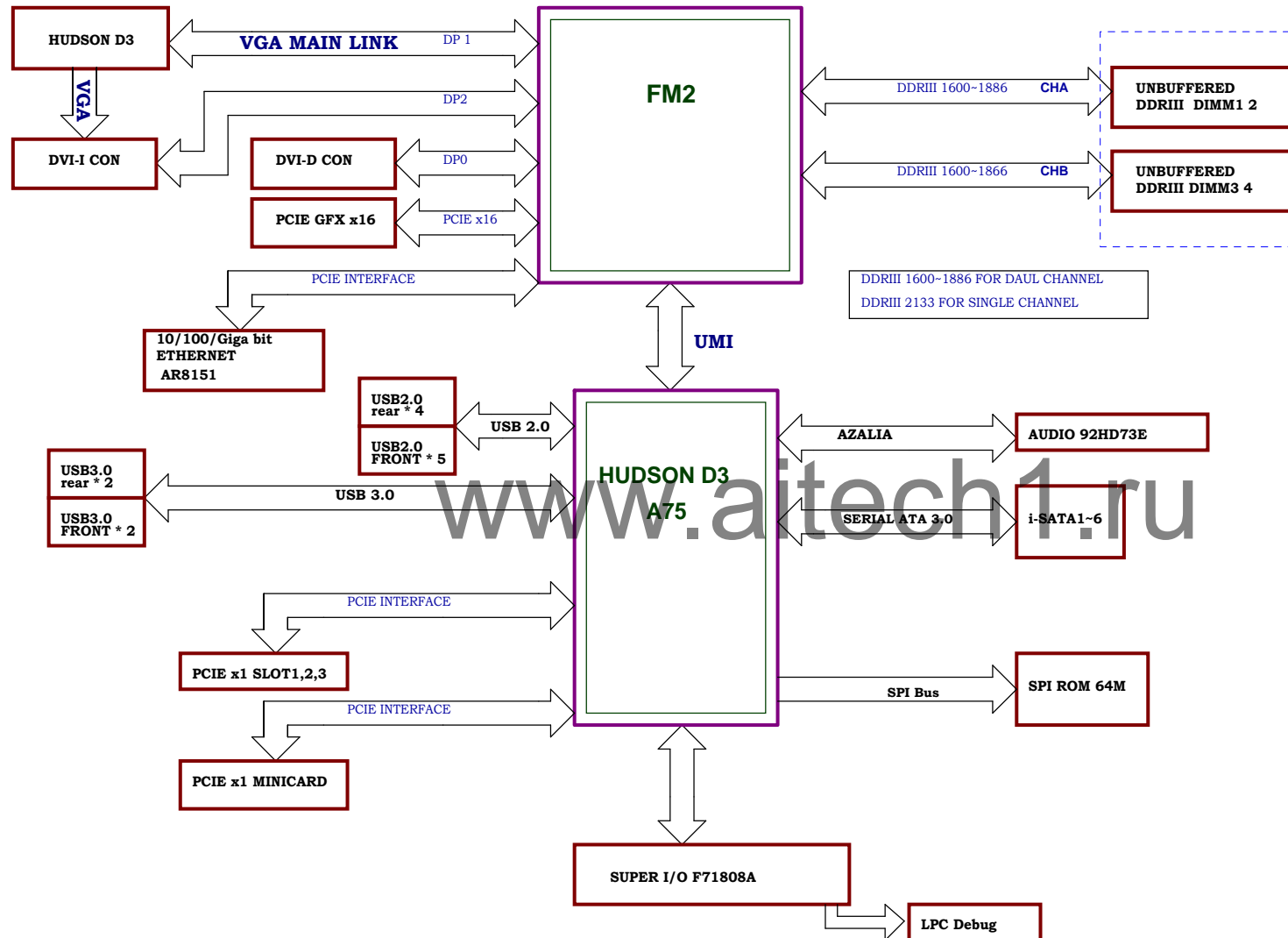
Cover Sheet

Rev
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Sheet 1 of 45

FUSION BLOCK DIAGRAM



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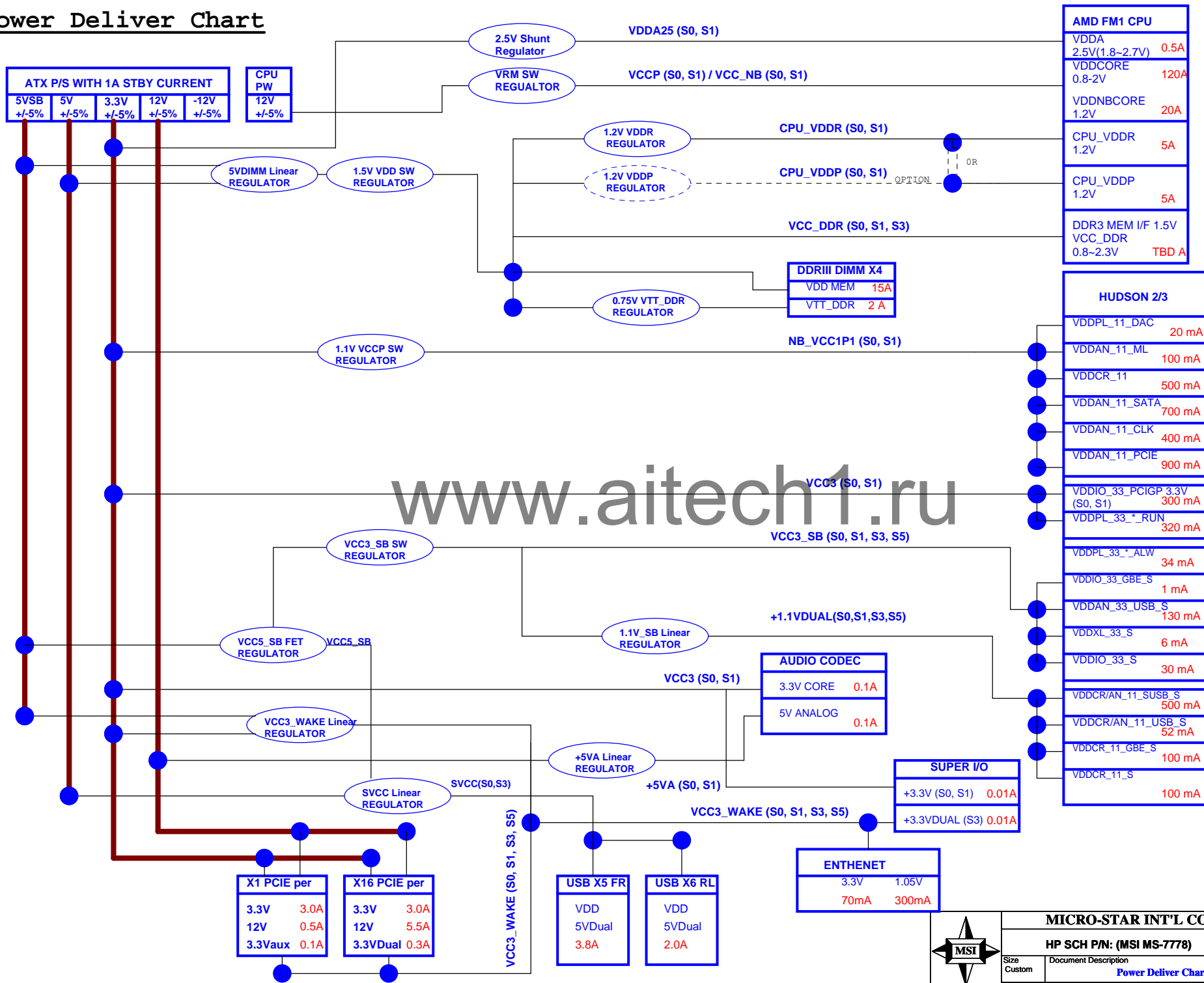
BLOCK DIAGRAM

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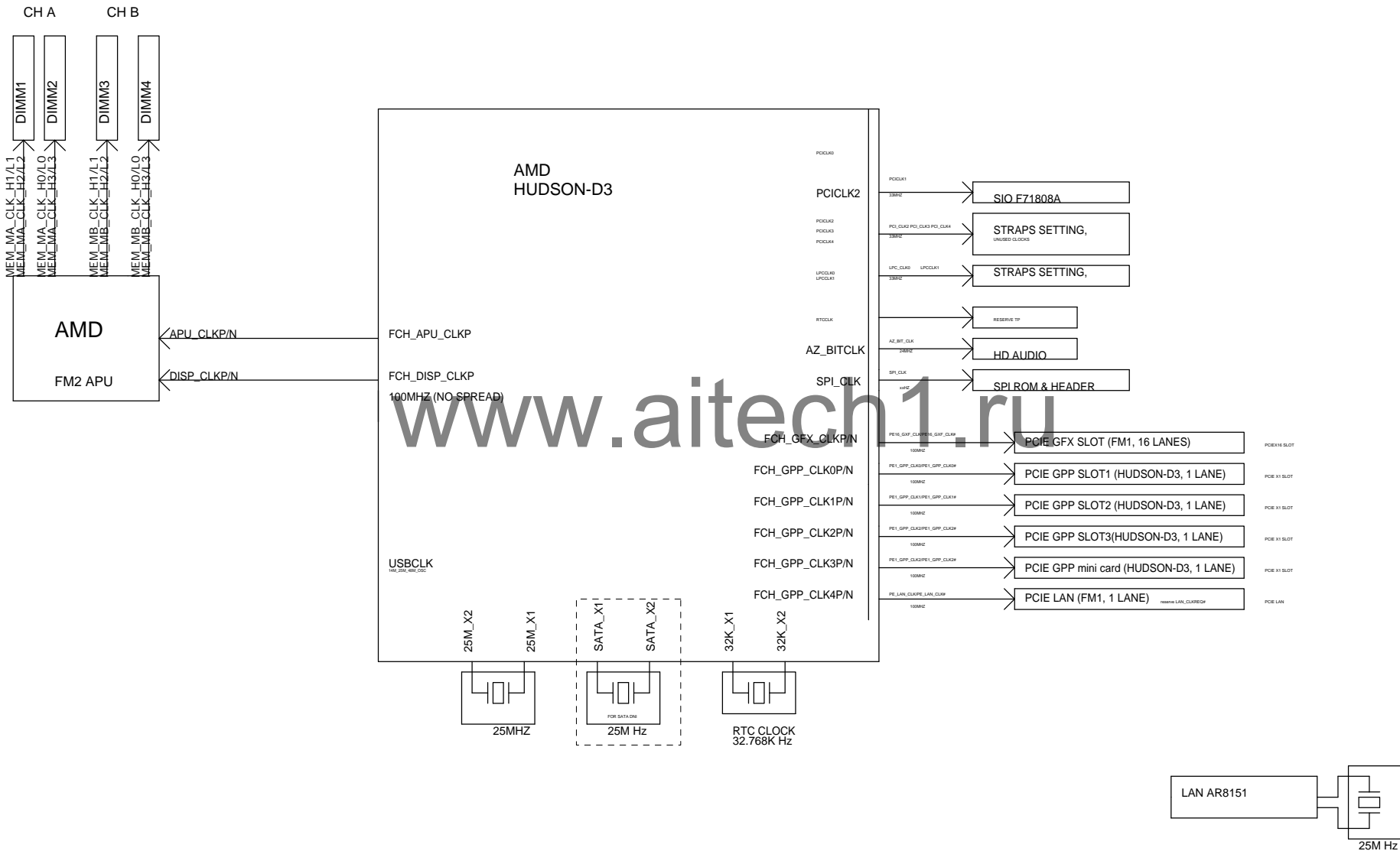
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Sheet 2 of 45

Power Deliver Chart

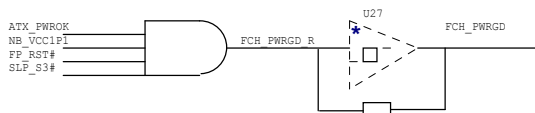
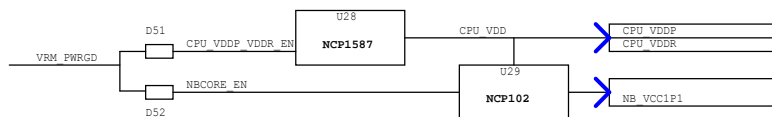
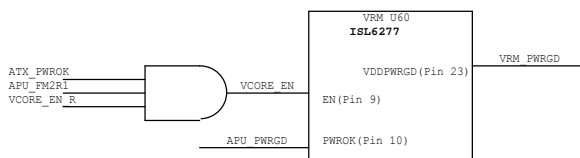
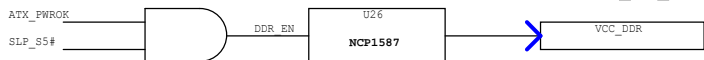
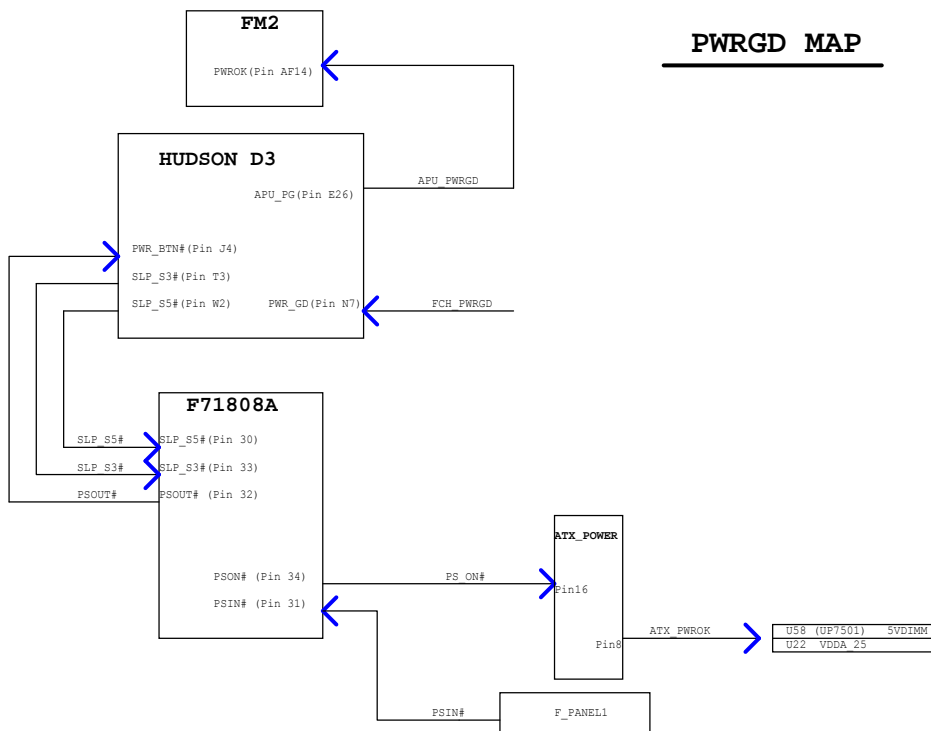


INTERNAL CLOCK MODE



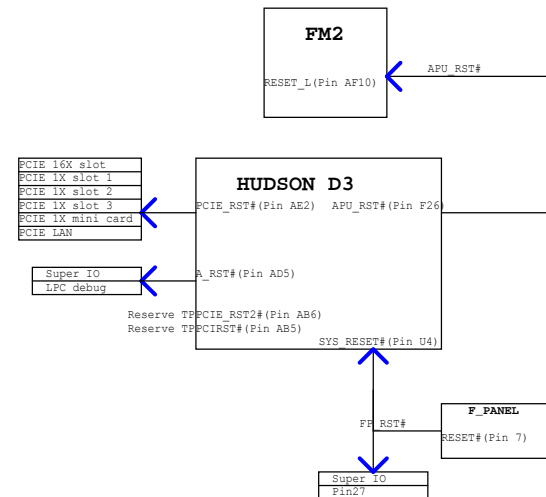
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Clock Distribution		
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PWRGD MAP



- * - MEANS OPTION

RESET MAP



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PWRGD&RESET Map

Rev
0A

Date:

Sheet 5 of 45

SUPER I/O F71808A GPIO Config

Pin	GPIO	Power Rail	Function description	Comment
20	GP22	VSB	POP_MUTE	
22	LEDVSB/GP24	VSB	LED1	
23	LEDVCC/GP25	VSB	LED_SW	
26	GP67	VSB	DEEP_S5	
53	GP00	VSB	EN_LD	
54	GP01	VSB	EN_HP	
55	GP02	VSB	EN_UVP	
58	GP05	VSB	FDO	
60	GP07	VSB	F_AUDIO_DET#	

FCH HUDSON D3 GPIO Config

Name	Pin	Function Description
GPIO0	AJ3	CLEAR CMOS
GPIO1	AL5	WLAN PWRON
GPIO2	AG4	USB20F1A
GPIO3	AL6	USB20F1B
GPIO4	AH3	USB20F2A
GPIO5	AJ5	USB20F2B
GPIO6	AL1	USB20F3
GPIO7	AN5	USB30FA
GPIO8	AN6	USB30FB
GPIO12	AM7	HW_ID1
GPIO13	AJ6	HW_ID2
GPIO14	AK7	HW_ID3
GPIO15	AN8	HW_ID4
GPIO23	AE21	STRAPPING
GPIO24	AC12	STRAPPING
GPIO25	AE13	STRAPPING
GPIO26	AF13	STRAPPING
GPIO27	AH13	STRAPPING
GPIO36	AF1	STRAPPING
GPIO38	AG2	STRAPPING
GPIO39	AF6	STRAPPING
GPIO42	AM17	STRAPPING
GPIO43	AD26	SMBus Clock 0
GPIO46	AK17	STRAPPING
GPIO47	AD25	SMBus Data 0
GPIO52	AH16	STRAPPING
GPIO67	AD22	SATA_LED
GPIO162	V3	SPI Clock
GPIO163	V5	SPI Data Out
GPIO164	V6	SPI Data In
GPIO165	T6	SPI Chip Select 1
GPIO170	Y1	HD Audio Serial Data
GPIO181	M1	LAN_ISOLATEB
GPIO199	J22	STRAPPING

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2
DIMM 2 CH-A	10100010B A4H	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H3/L3
DIMM 3 CH-B	10100001B A2H	MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H3/L3

SMBus TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
APU	DPO_AUXP_C /DPO_AUXN_C	DVI
	DP1_AUXP_C /DP1_AUXN_C	Hudson D3 DP to VGA translator
FCH	SCLK0/SDATA0	DIMMs,CLOCK GEN ,SIO
	SCLK1/SDATA1	LAN,PCIE SLOTS,MINI_PCIE
	SCLK3/SDATA3	TP

RESET TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
FCH	PCIE_RST#	PCie 16X,1X,LAN,MINI_PCIE
	A_RST#	SIO,LPC debug
	PCIE_RST2#	RESERVE TP
	LDT_RST#	APU
	AZ_RST#	AZALIA CODEC
	DDR3_RST#	NC
	FC_RST#	DEBUG BUS
	ROM_RST#	NC
FRONT PANEL	FP_RST#	FCH,CLOCK GEN

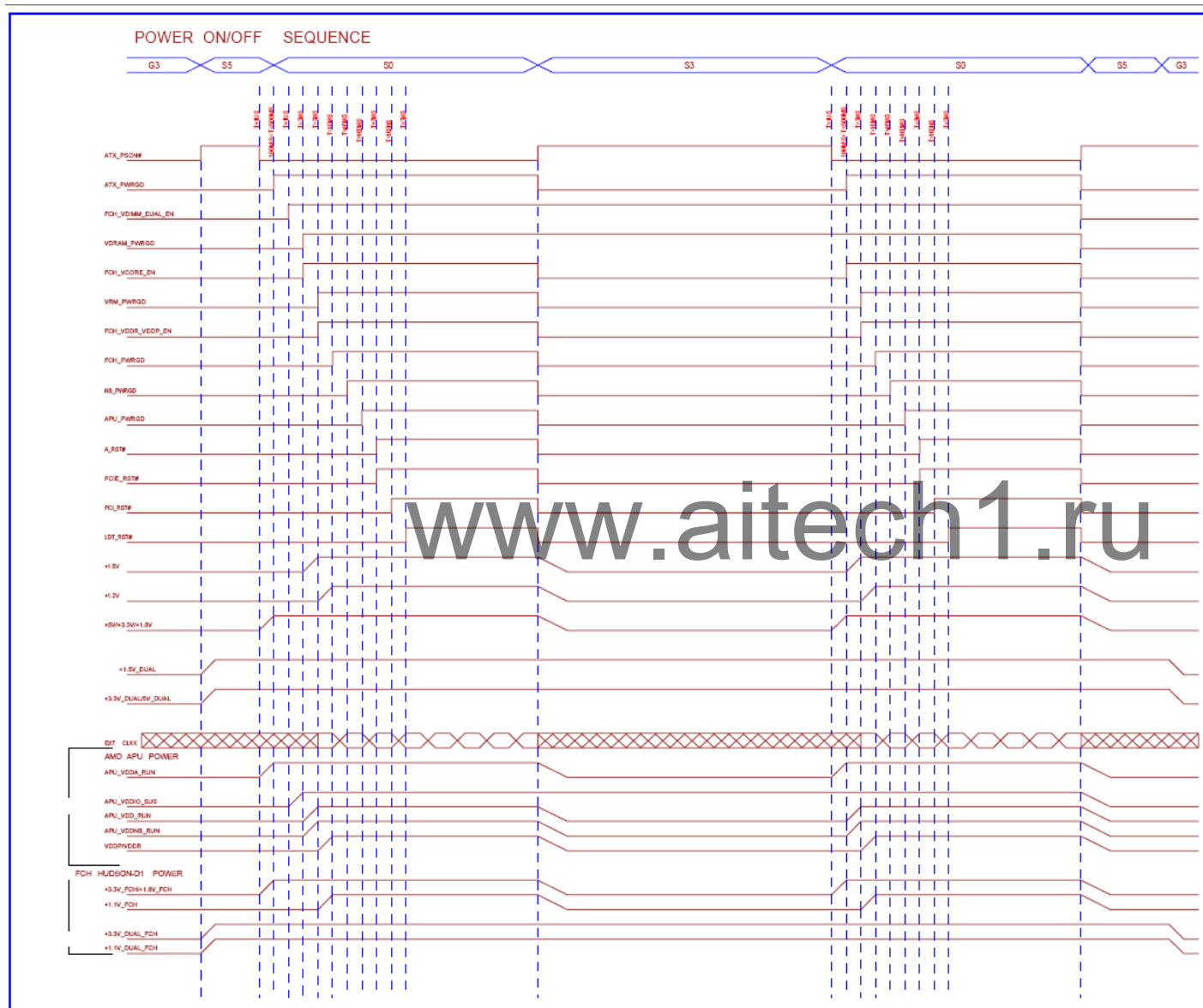


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POWER ON SEQUENCE



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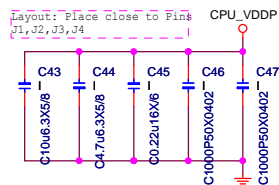
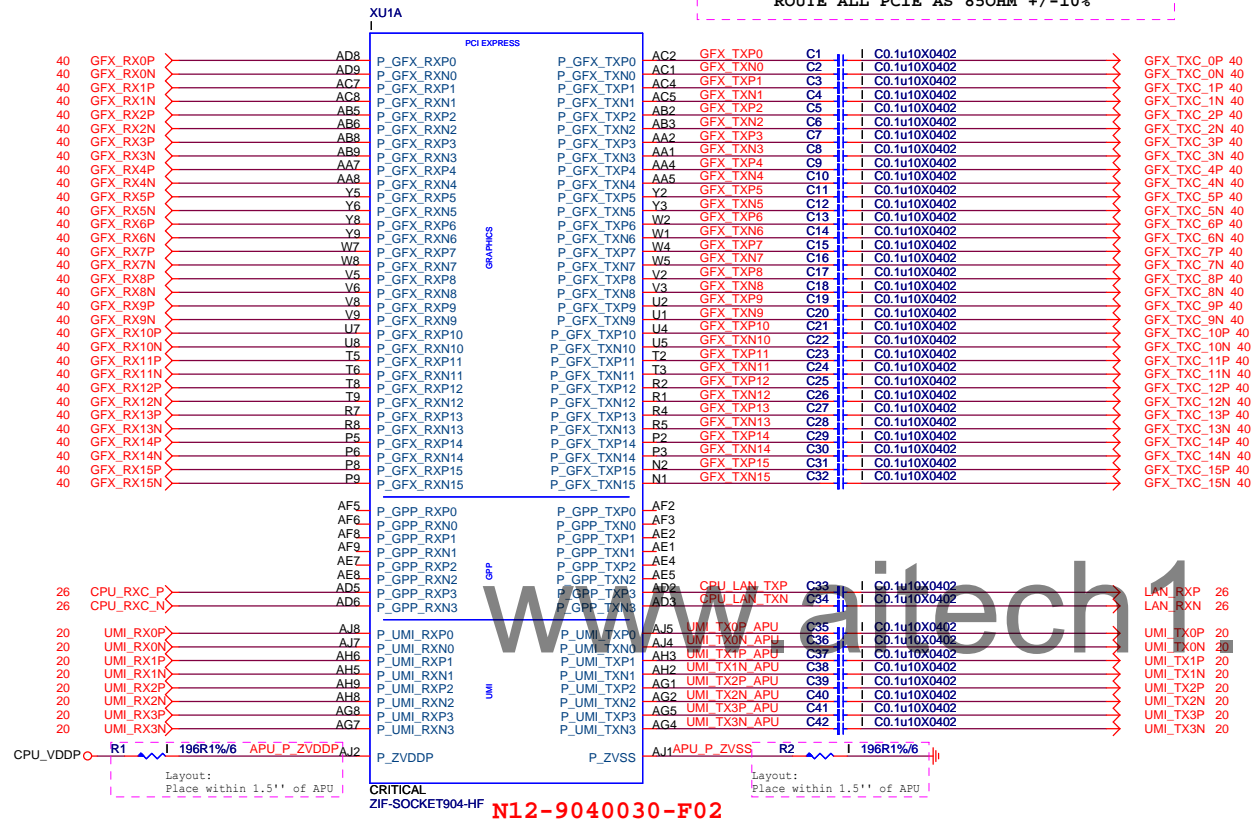
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Sheet 7 of 45

FM2 PCIE I/F

```
mach@CRB PCIe AC Capacitors:75nF to 200nF
      Layout: PLACE CAPS WITH APU < 1 INCH
      ROUTE ALL PCIe AS 85OHM +/-10%
```



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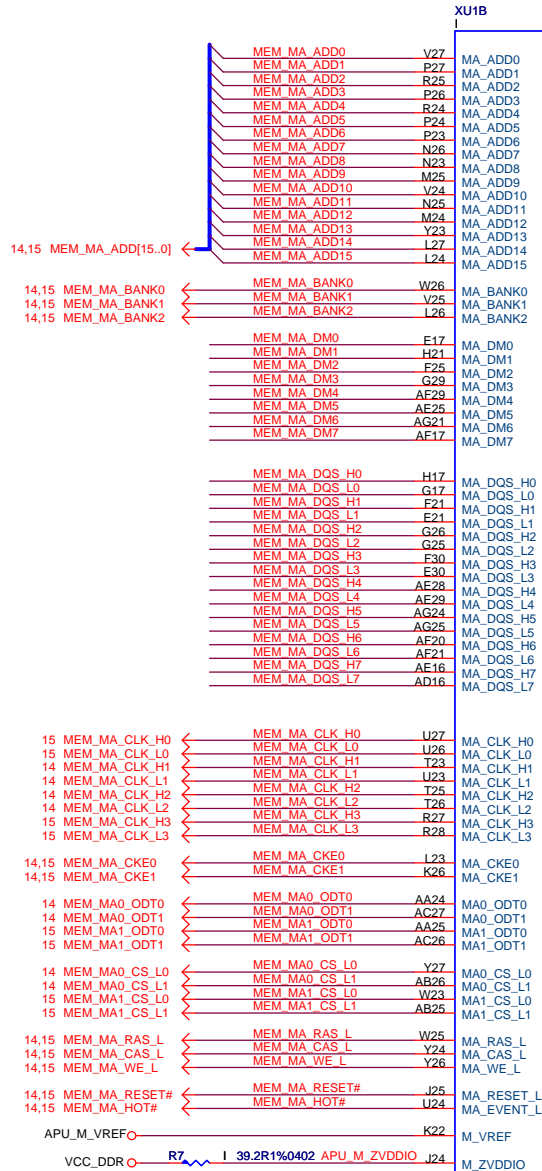
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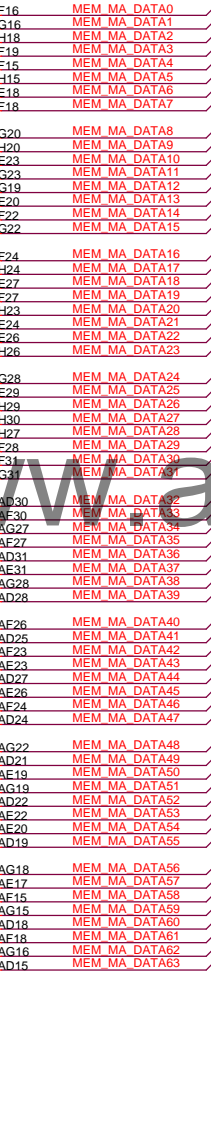
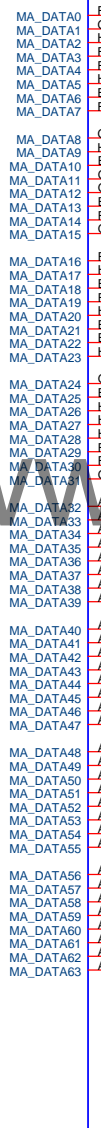
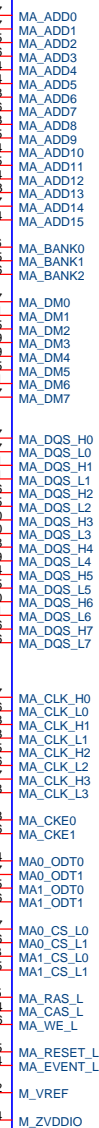
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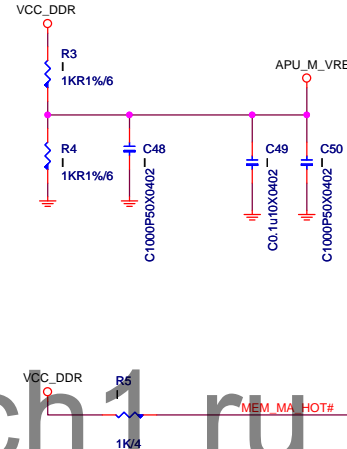
14,15 MEM_MA_DQS_L[7..0] <-->
14,15 MEM_MA_DQS_H[7..0] <-->
14,15 MEM_MA_DM[7..0] <-->



XU1B



MEM_MA_DATA[63..0] 14,15



CRITICAL
ZIF-SOCKET904-HF

N12-9040030-F02



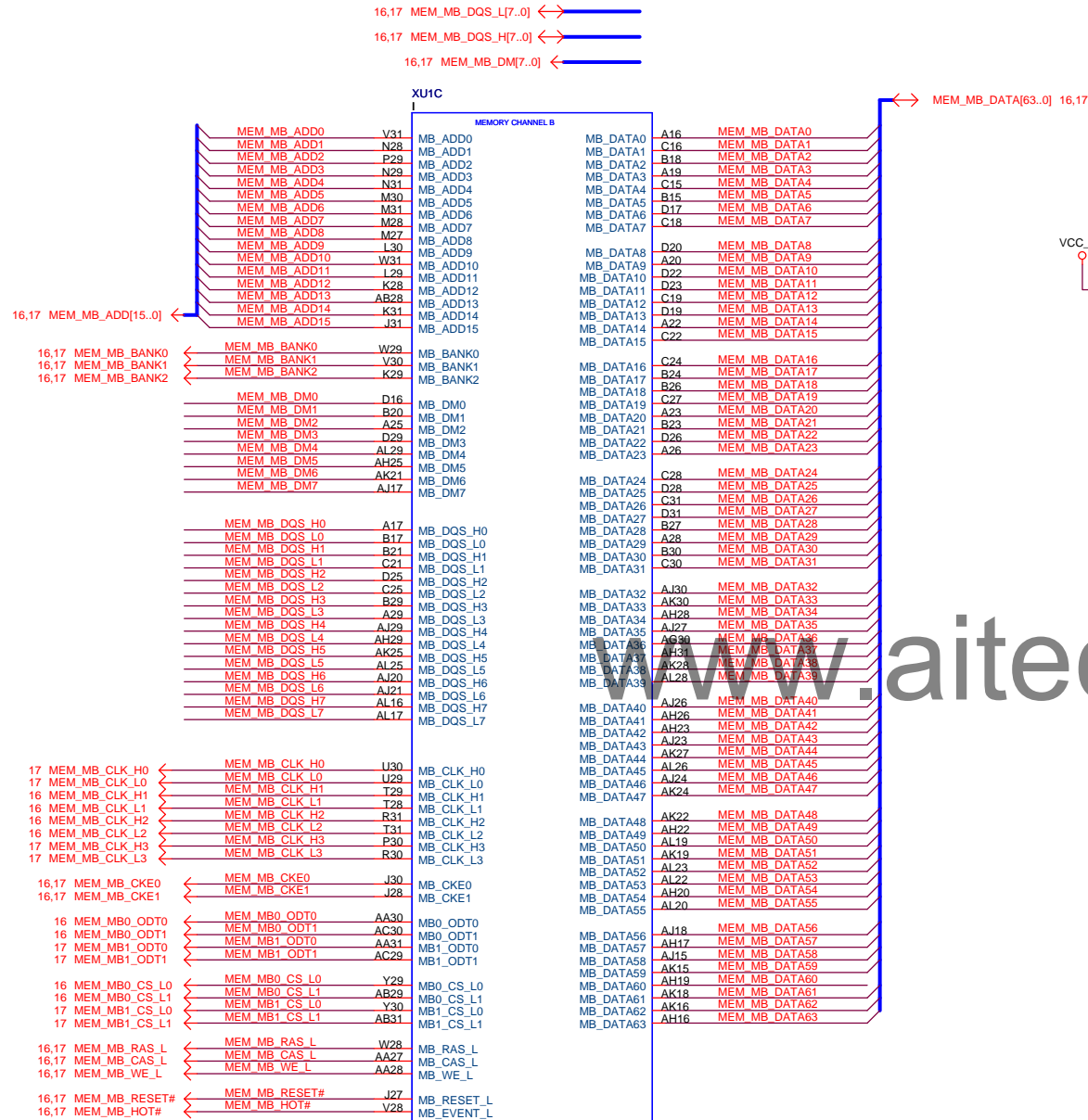
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

Document Description

FM2 DDR3 I/F(A)

Date: Sheet 9 of 45



CRITICAL
ZIF-SOCKET904-HF

N12-9040030-F02



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FM2 DDR3 I/F(B)

Rev
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Date:

Sheet 10 of 45

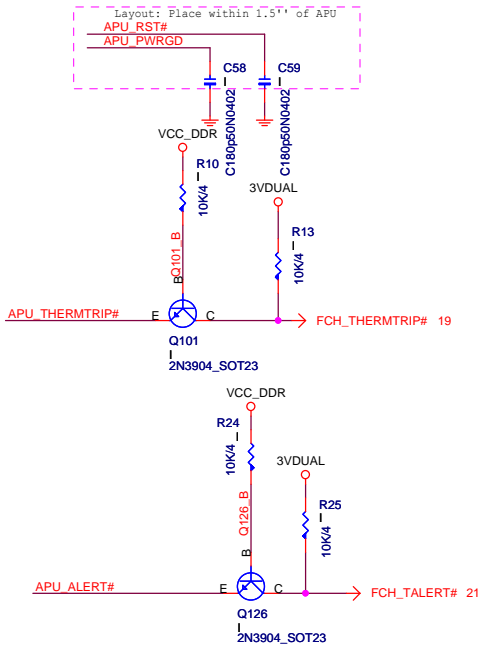
FM1 DISPLAY I/F

Note: Several vias on the DP0 interface violate the minimum distance rules for via to via spacing between diff pairs. These violations have been reviewed and approved on an individual basis, and pose no significant signal integrity issues for this implementation since the route lengths are under the maximum allowed spec, and the via distance violations are not severe.

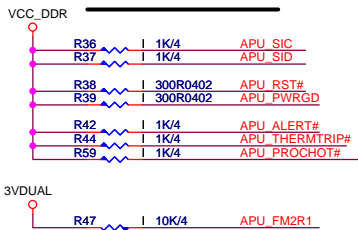
ROUTE PCIE AS 850HM +/-10%

PLACE CAPS WITH APU < 1 INCH

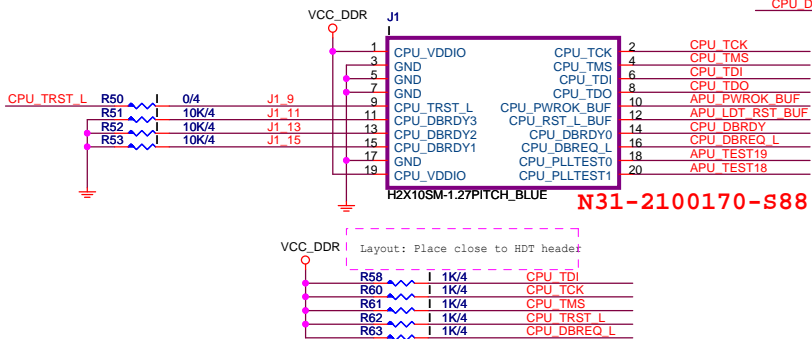
Trace length within 10"



PULL UP



HDT+ Connector



XU1D

ANALOG/DISPLAY/MISC

DP0_TXP0
DP0_TXN0

DP0_TXP1
DP0_TXN1

DP0_TXP2
DP0_TXN2

DP0_TXP3
DP0_TXN3

DP1_TXP0
DP1_TXN0

DP1_TXP1
DP1_TXN1

DP1_TXP2
DP1_TXN2

DP1_TXP3
DP1_TXN3

DP2_TXP0
DP2_TXN0

DP2_TXP1
DP2_TXN1

DP2_TXP2
DP2_TXN2

DP2_TXP3
DP2_TXN3

DP2_TXP4
DP2_TXN4

DP2_TXP5
DP2_TXN5

DP2_TXP6
DP2_TXN6

CLKIN_H
CLKIN_L

DISP_CLKIN_H
DISP_CLKIN_L

APU_SVC_R
APU_SVC_R

APU_SVD_R
APU_SVD_R

APU_SVT_R
APU_SVT_R

APU_RST#
APU_RST#

APU_PWRGD
APU_PWRGD

APU_PROCHOT#
APU_PROCHOT#

APU_THERMTRIP#
APU_THERMTRIP#

APU_ALERT#
APU_ALERT#

CPU_TDI
CPU_TDI

CPU_TCK
CPU_TCK

CPU_TMS
CPU_TMS

CPU_TRST_L
CPU_TRST_L

CPU_DBRDY
CPU_DBRDY

CPU_DBREQ_L
CPU_DBREQ_L

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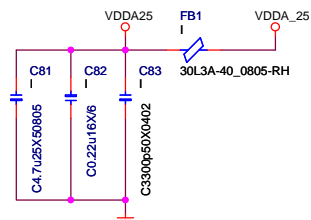
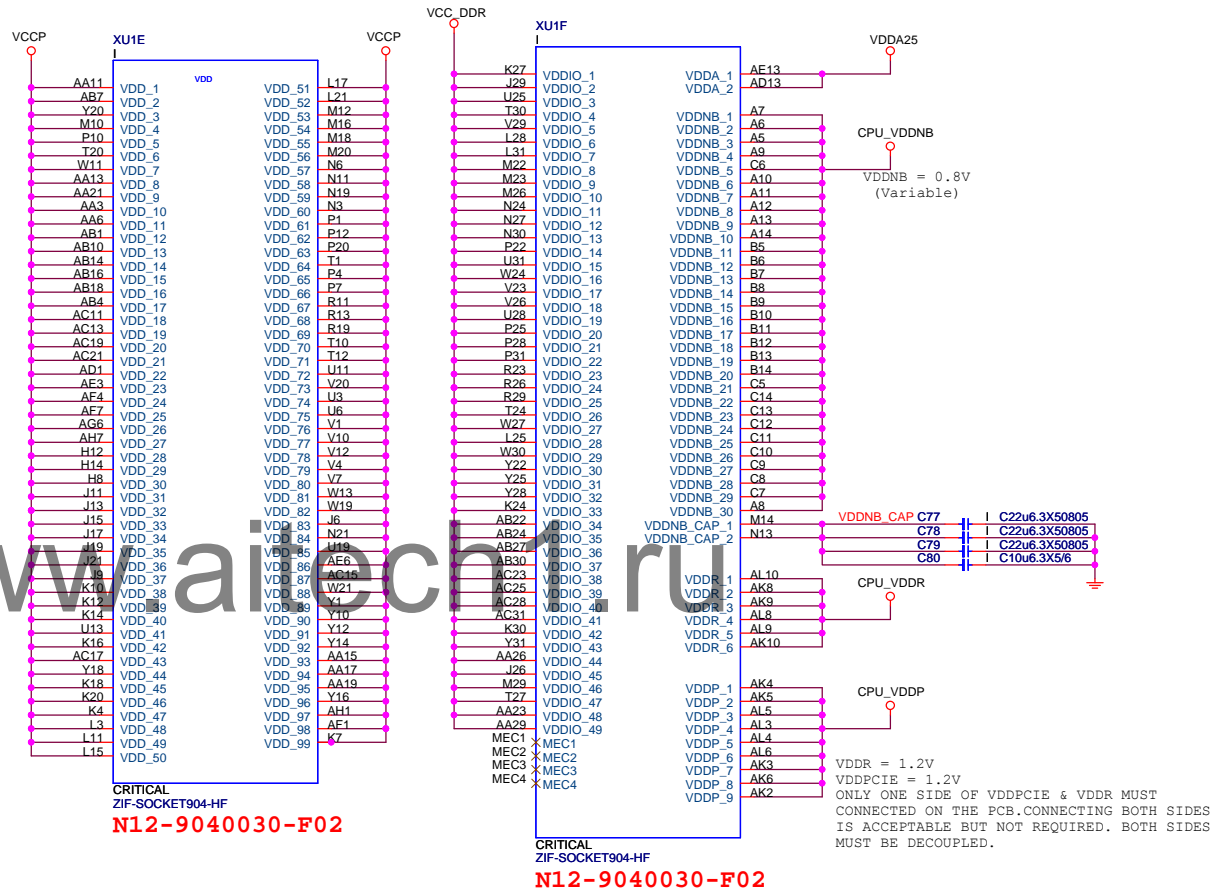
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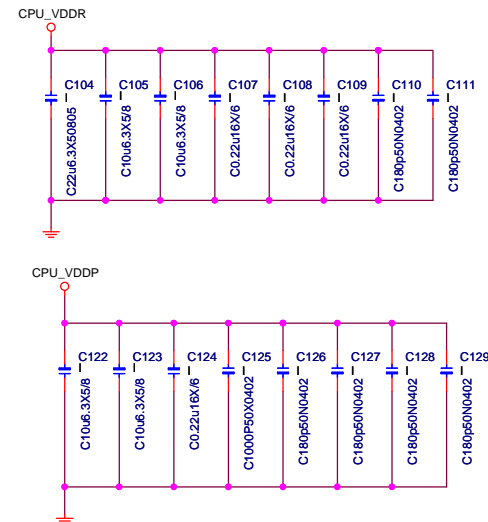
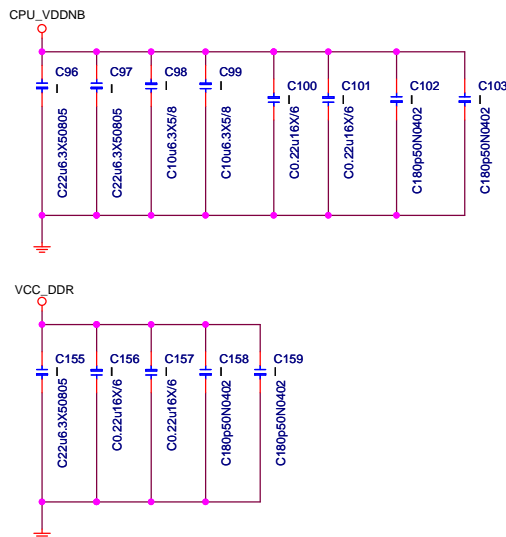
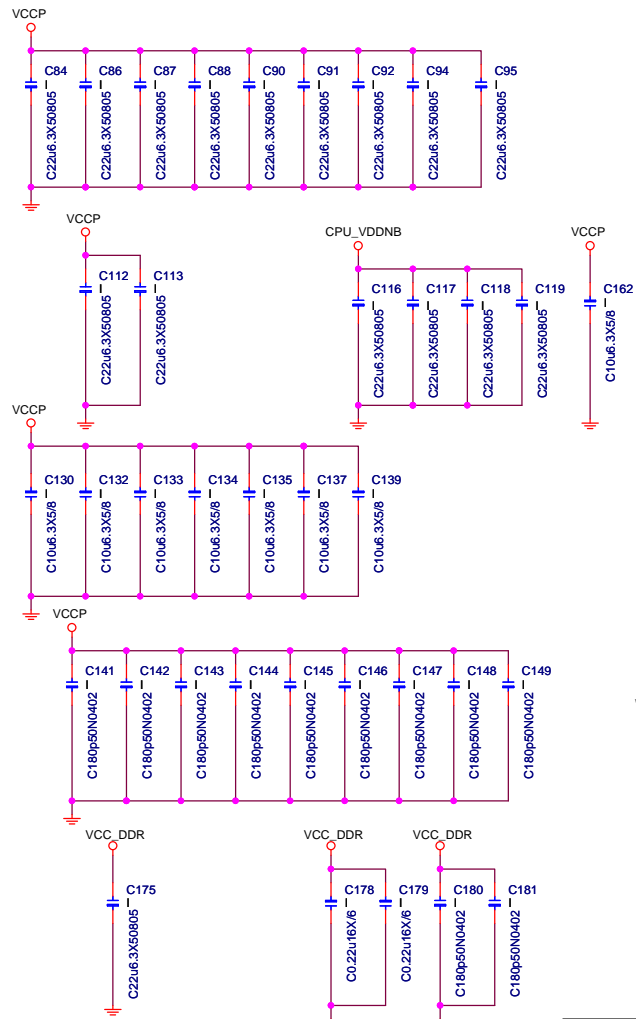


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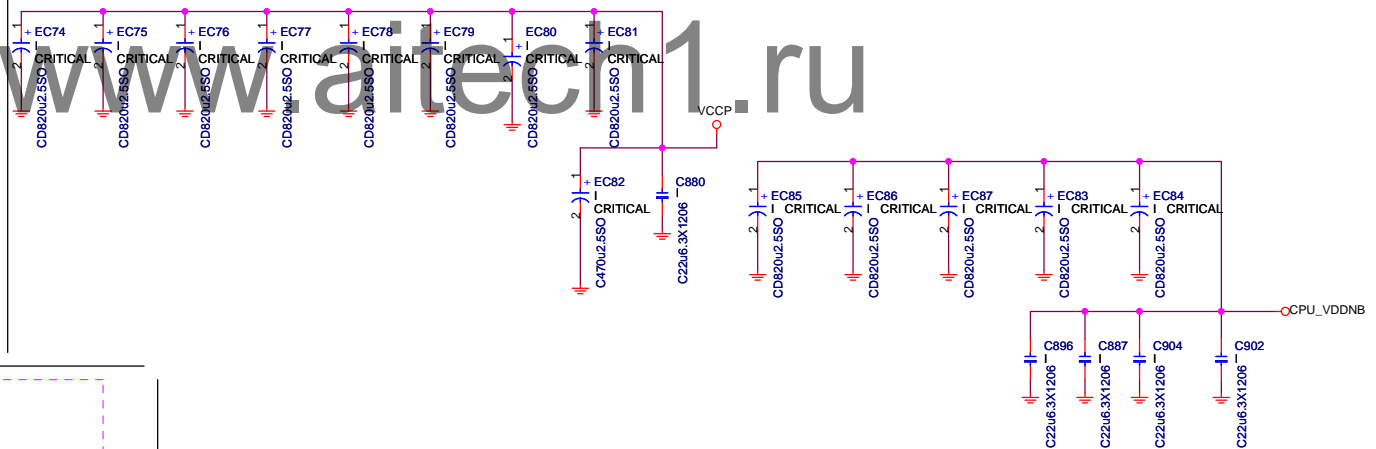
HP SCH P/N: (MSI MS-7778)

Size Custom	Document Description	Rev 0A
	FM2 POWER/GND	
Date:	Sheet 12 of 45	

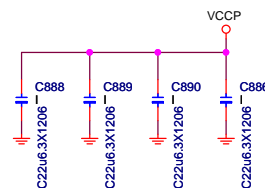
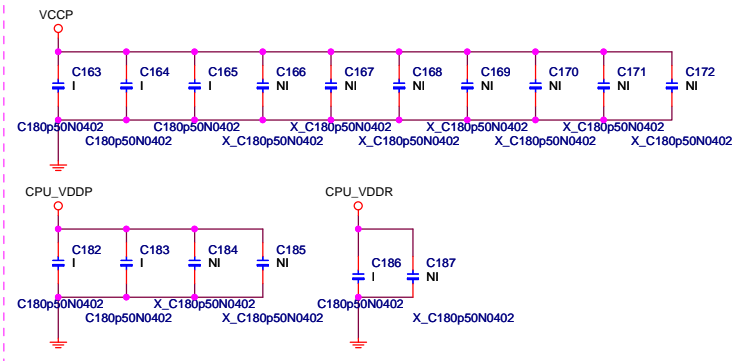
CPU POWER CAPS



VCORE CAPS



EMC Caps On Bottom side



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HP SCH P/N: (MSI MS-7778)


Size	Document Description	Rev
Custom	FM2 CAPS & VCORE CAP	0A
Date:	Sheet 13 of 45	

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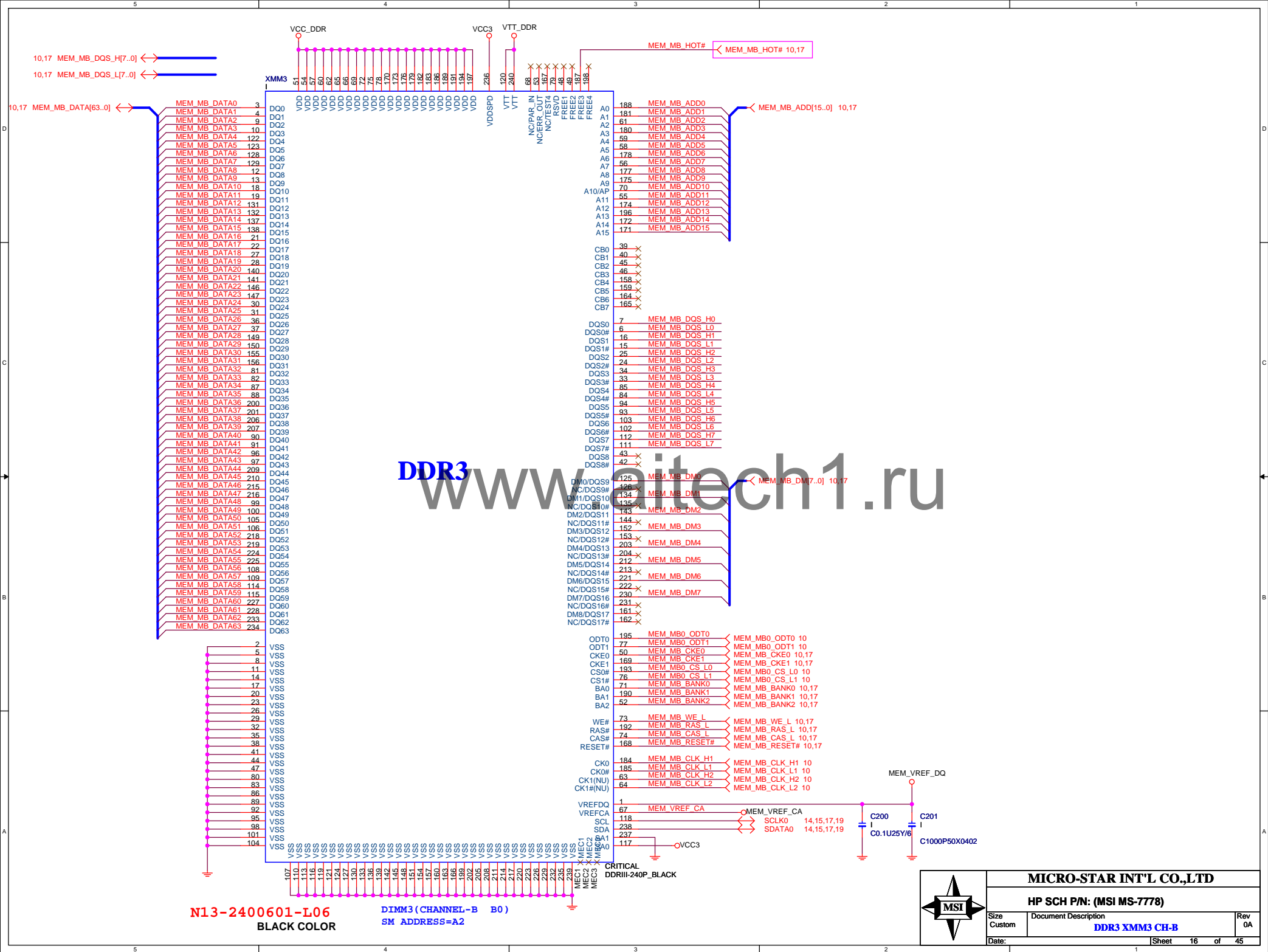
DDR3

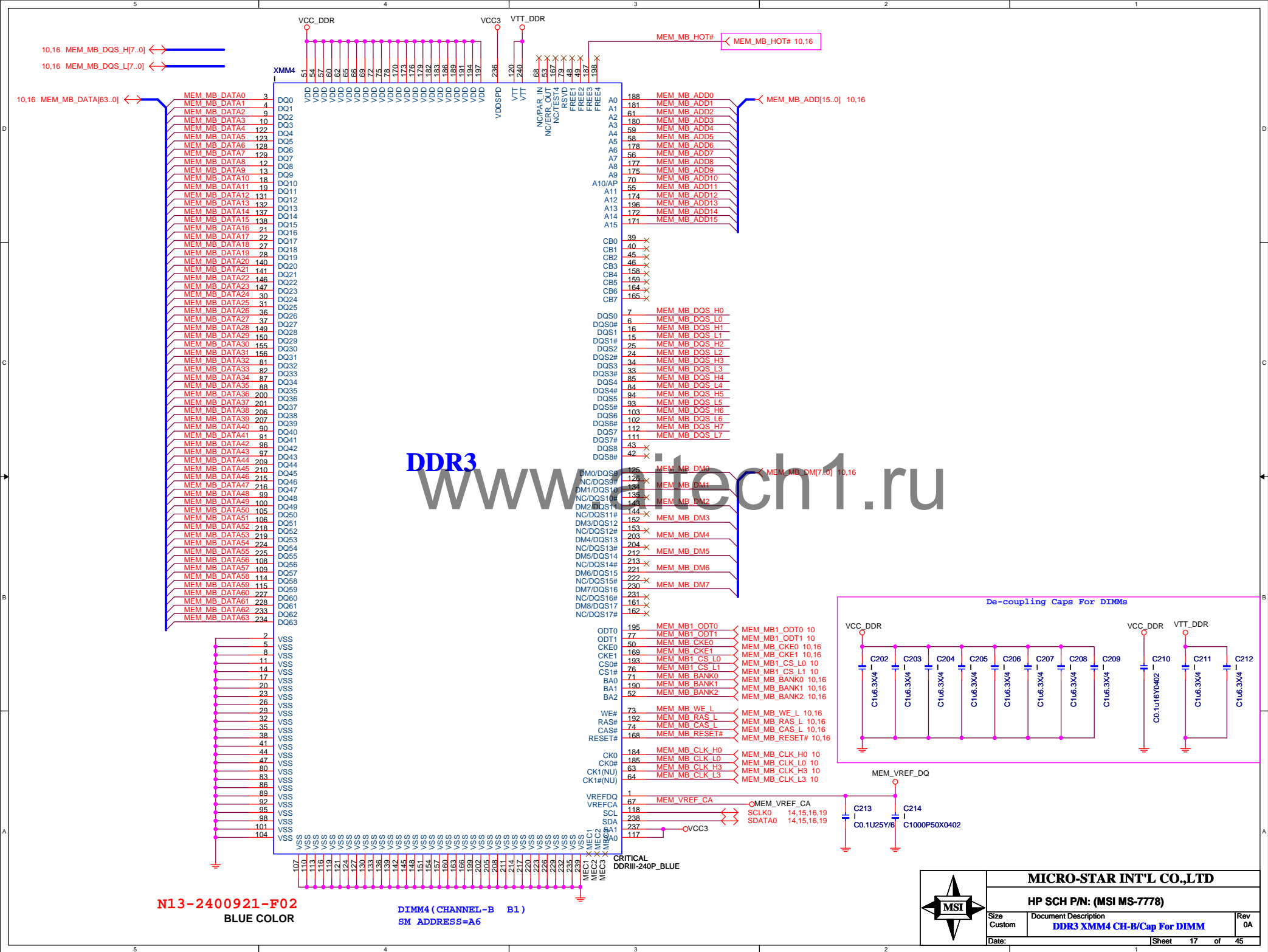
N13-2400921-L06
BLUE COLOR

DIMM2 (CHANNEL-A A1)
SM ADDRESS=A4

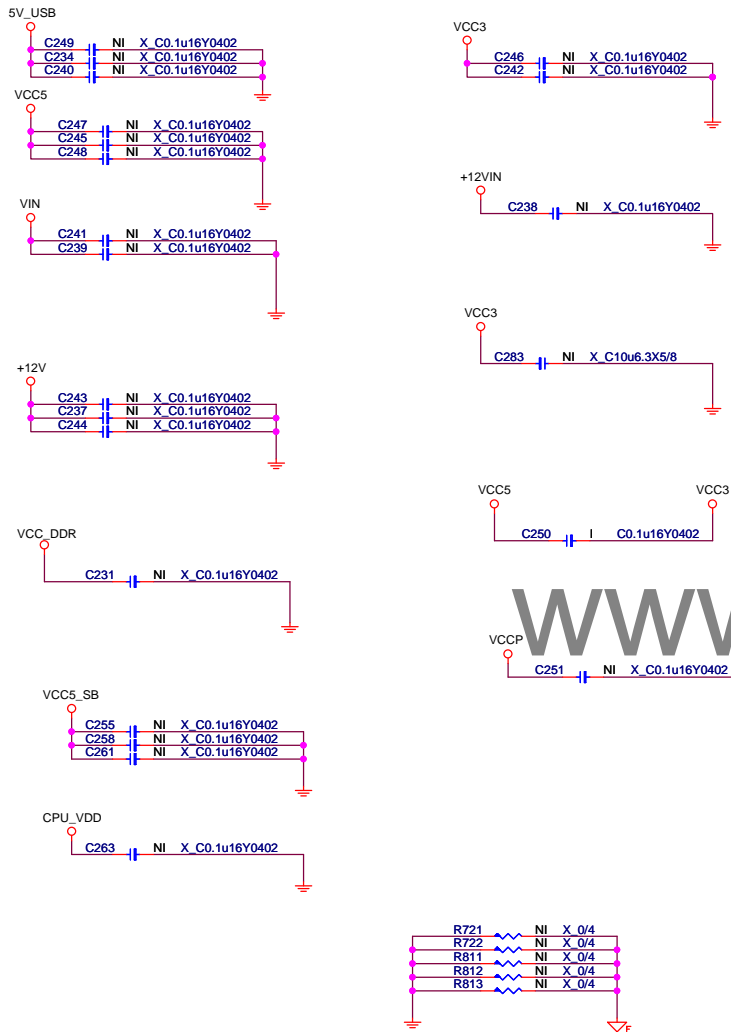


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HP SCH P/N: (MSI MS-7778)		
Size Custom	Document Description	Rev 0A
DDR3 XMM2 CH-A		
Date:	Sheet 15	of 45





EMI Reserved

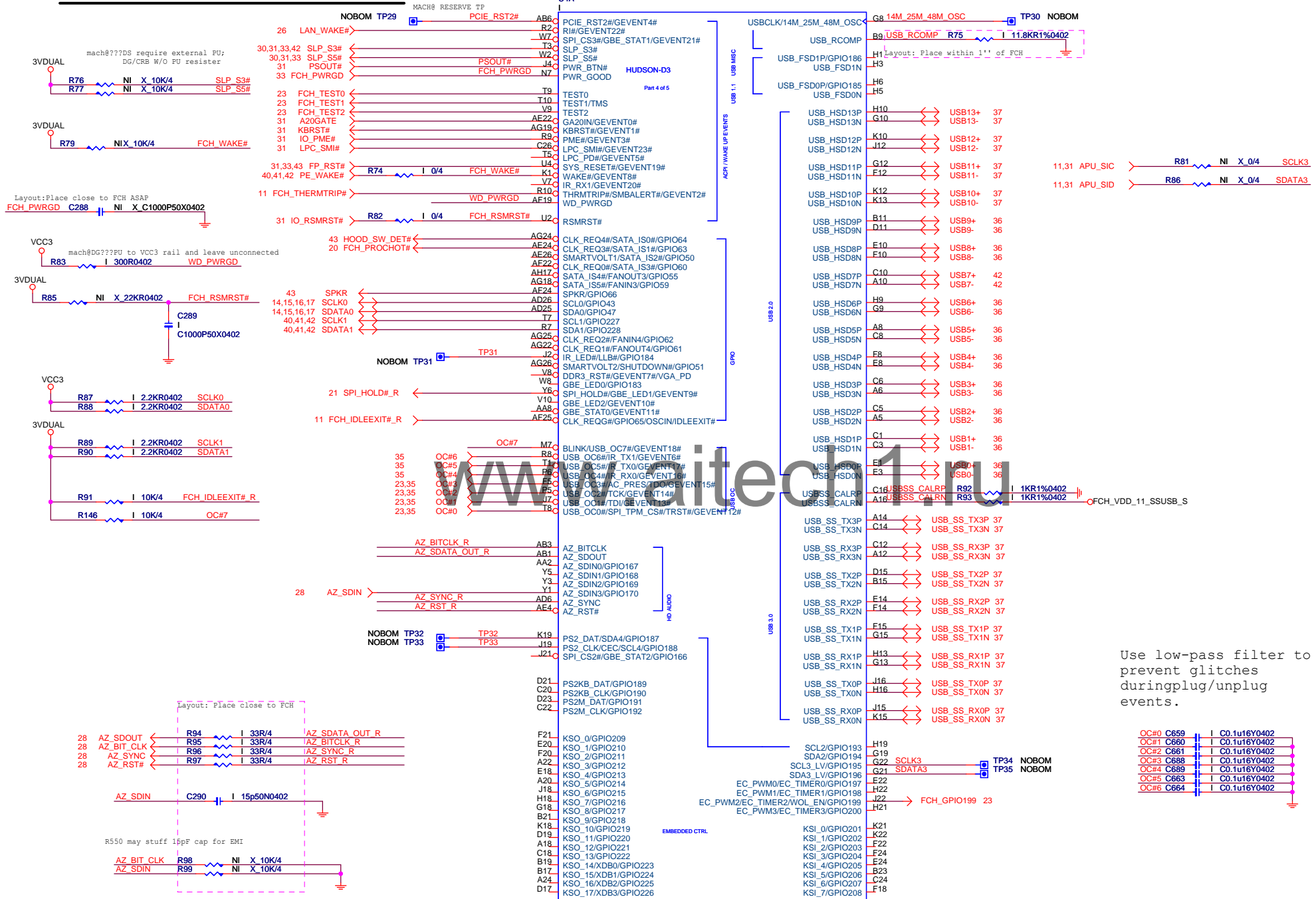


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HP SCH P/N: (MSI MS-7778)		
Size Custom	Document Description EMI Reserved	Rev 0A
Date:	Sheet 18 of 45	

HUDSON ACPI/USB/AZ/GPIO



Use low-pass filter to prevent glitches during plug/unplug events.

OC#0 C859 I C0.1u16Y0402
OC#1 C860 I C0.1u16Y0402
OC#2 C861 I C0.1u16Y0402
OC#3 C888 I C0.1u16Y0402
OC#4 C889 I C0.1u16Y0402
OC#5 C663 I C0.1u16Y0402
OC#6 C664 I C0.1u16Y0402



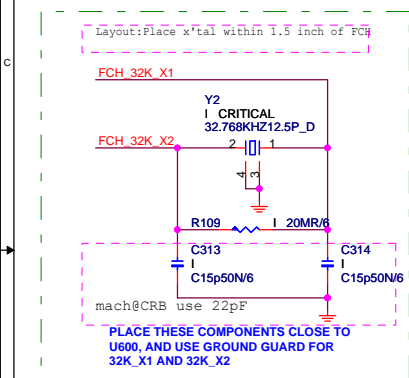
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

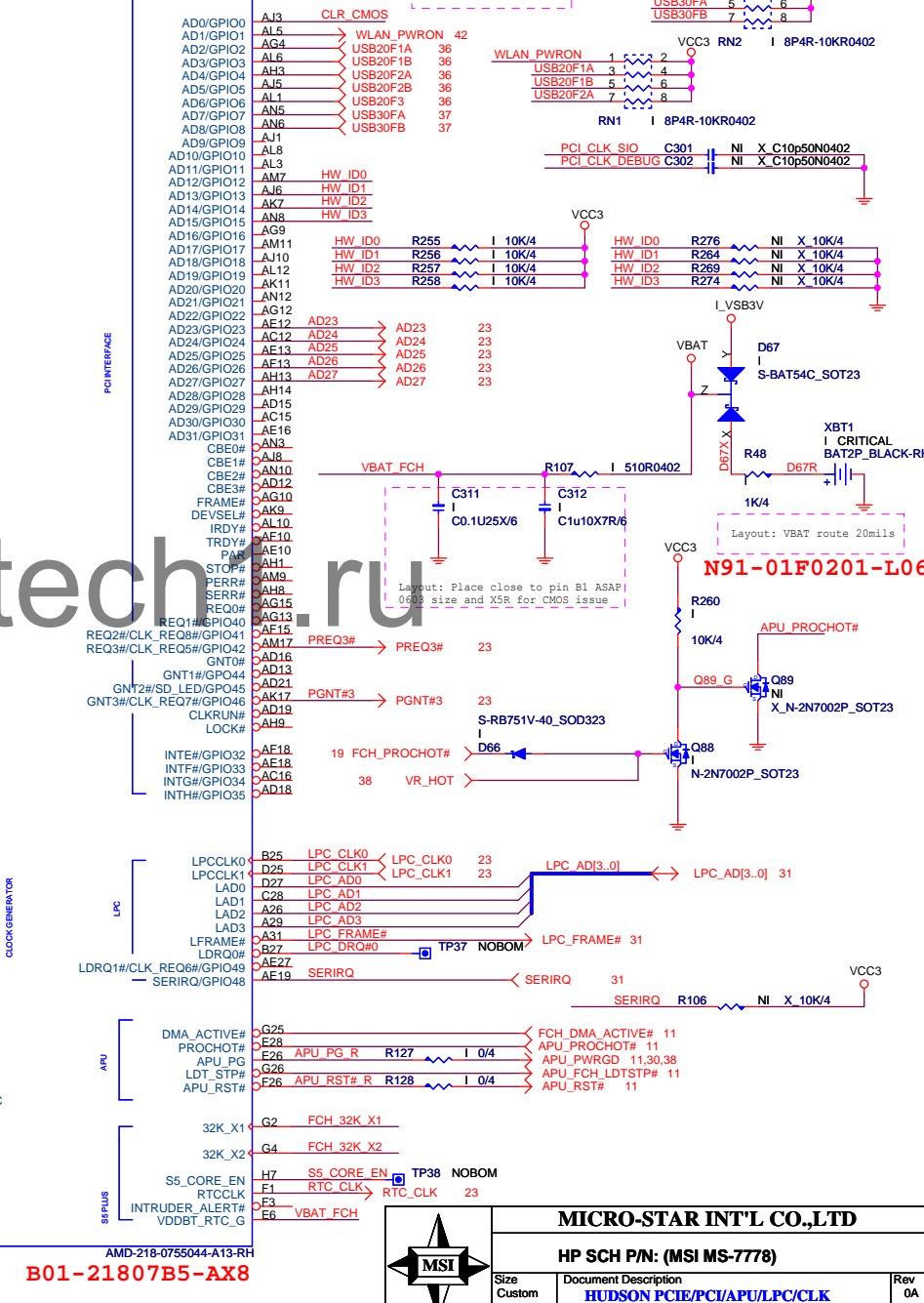
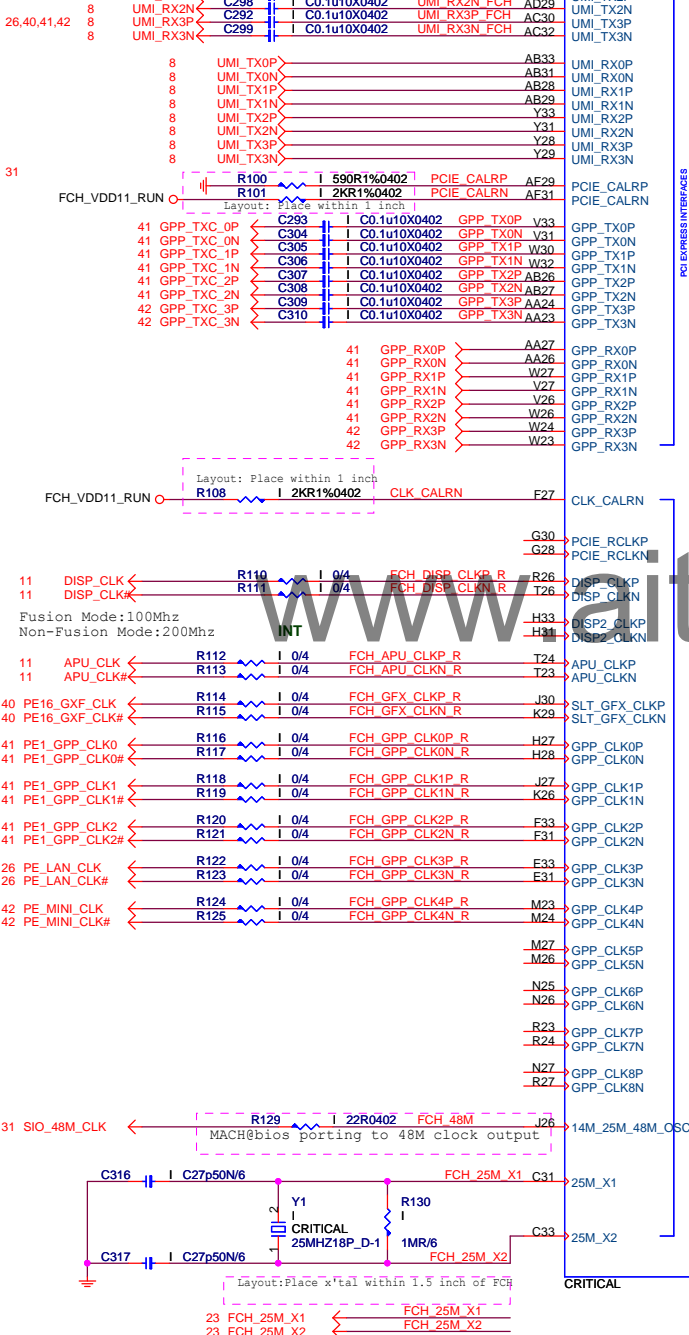
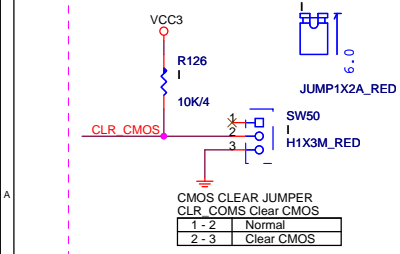
Size	Document Description	Rev
Custom	HUDSON ACPI/USB/AZ/GPIO	0A
Date:	Sheet 19 of 45	

B01-21807B5-AX8

```
A_RST# for LPC device;
PCIE_RST# for APU PCIE device;
PCIE_RST#2 FCH PCIE device
```



N31-1030211-H06



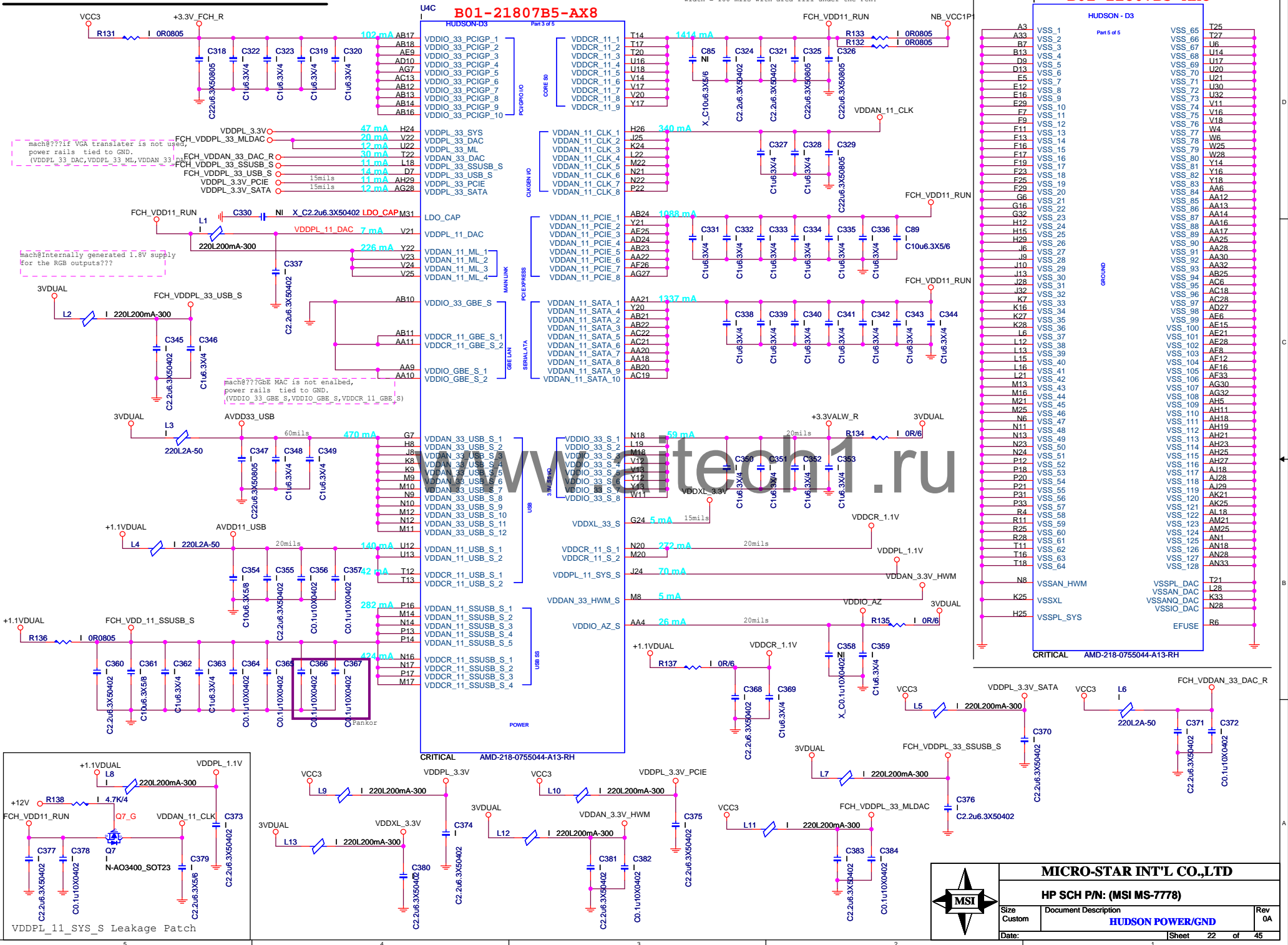
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

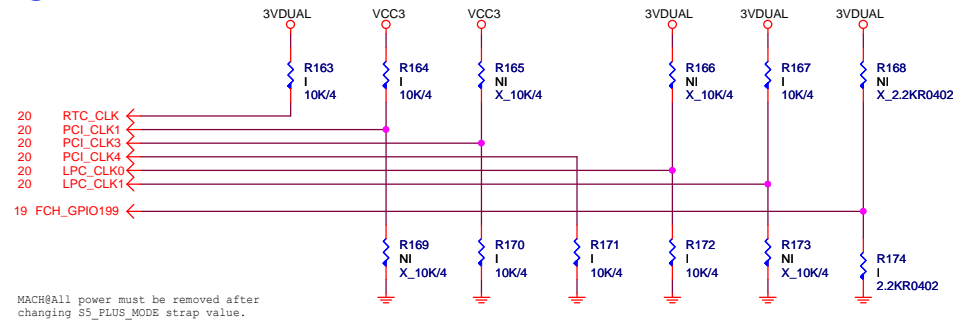
Document Description
HUDSON PCIE/PCI/USB/LPC/CL

Size Custom	Document Description HUDSON PCIE/PCI/APU/LPC/CLK	Rev 0
Date:	Sheet 20 of 45	

HUDSON POWER&DECOUPLING



FCH REQUIRED STRAPS



	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	S5 PLUS MODE DISABLED DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	Reserved	EC ENABLED	INTERNAL CLOCK GEN ENABLED DEFAULT	LPC ROM
PULL LOW	S5 PLUS MODE ENABLED	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Required setting for intergrated CLOCK MODE DEFAULT	EC DISABLED DEFAULT	INTERNAL CLOCK GEN DISABLED	SPI ROM DEFAULT

FCH DEBUG STRAPS

Provided test point access for lab use.
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

NOBOM TP42 AD27 → AD27 20
NOBOM TP43 AD26 → AD26 20
NOBOM TP45 AD25 → AD25 20
NOBOM TP47 AD24 → AD24 20
NOBOM TP48 AD23 → AD23 20

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK Termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL DOWN	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH XOR CHAIN TEST

NOBOM TP41 → FANOUT0 21 FCH XOR CHAIN OUTPUT
NOBOM TP44 → FCH_25M_X1 20 FCH XOR CHAIN REF CLOCK
NOBOM TP46 → FCH_25M_X2 20

NOBOM TP49 → FCH_TEST0 → FCH_TEST0 19
NOBOM TP50 → FCH_TEST2 → FCH_TEST2 19

TEST2	TEST1	TEST0	Description
0	1	X	Enable test mode

3VDUAL → R175 NI X_2.2KR0402 → FCH_TEST1 19 SHORTING PLUG

FCH PCIE EEPROM STRAPS

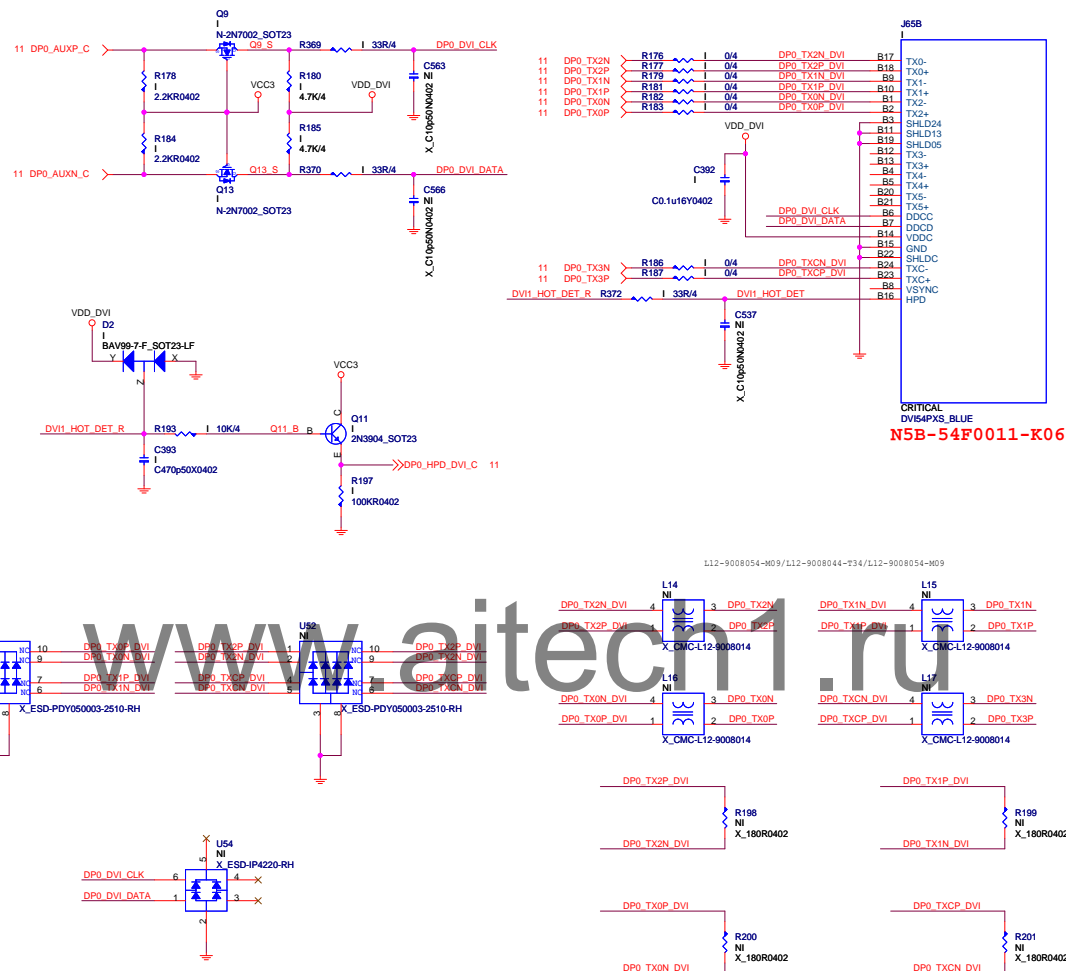
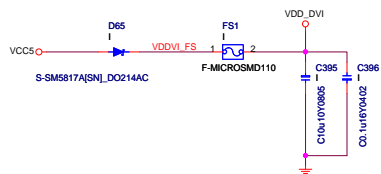
NOBOM TP52 → PREQ3# → PREQ3# 20
NOBOM TP54 → PGNT3# → PGNT3# 20

FCH ICE DEBUG /JTAG TEST PINS

NOBOM TP51 → FCH_TEST → FCH JTAG TMS
NOBOM TP53 → OC#0 → FCH JTAG TRST# OC#0 19,35
NOBOM TP55 → OC#1 → FCH JTAG TDI OC#1 19,35
NOBOM TP56 → OC#2 → FCH JTAG TCK OC#2 19,35
NOBOM TP57 → OC#3 → FCH JTAG TDO OC#3 19,35



DVI POWER

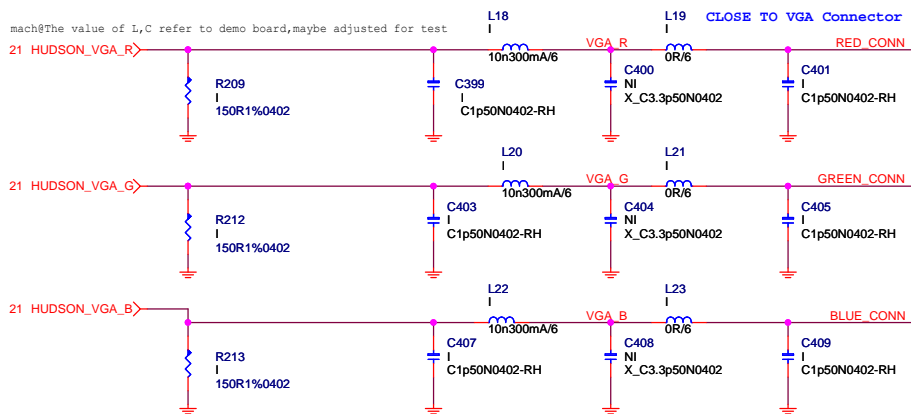
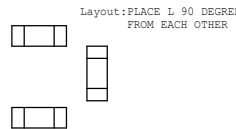


HP SCH P/N: (MSI MS-7778)

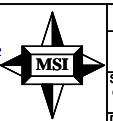
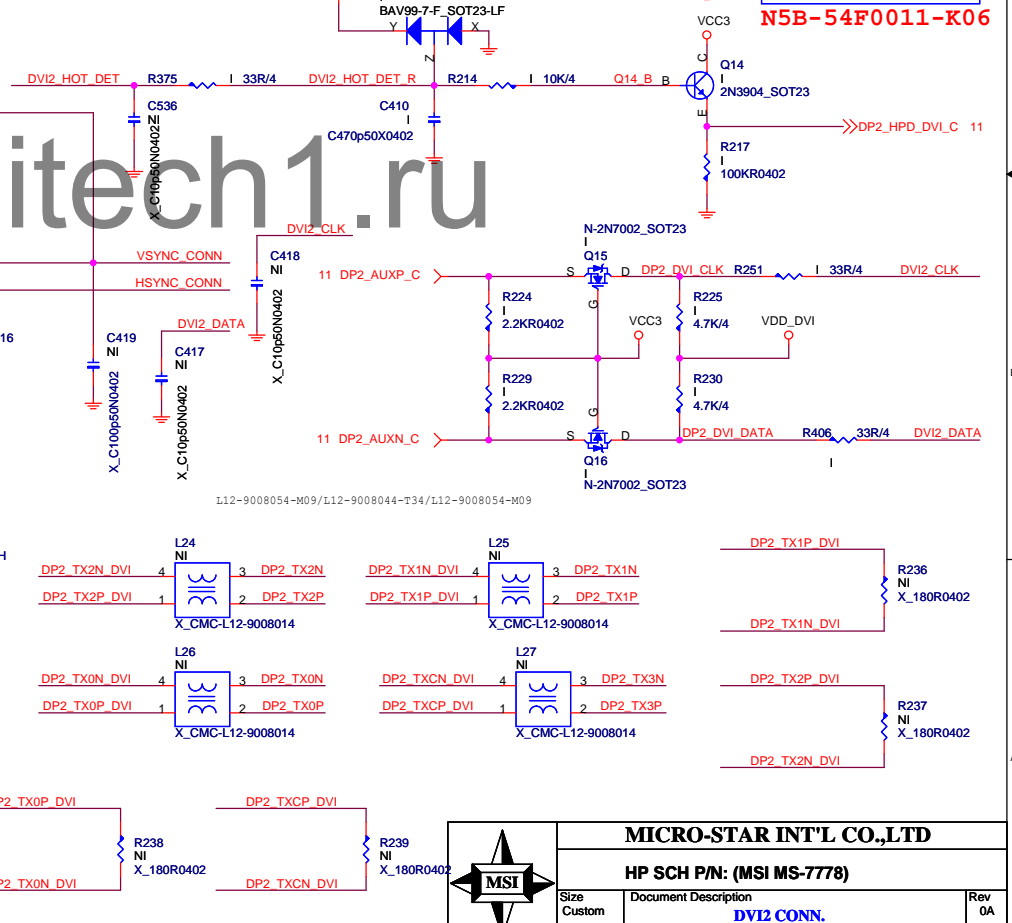
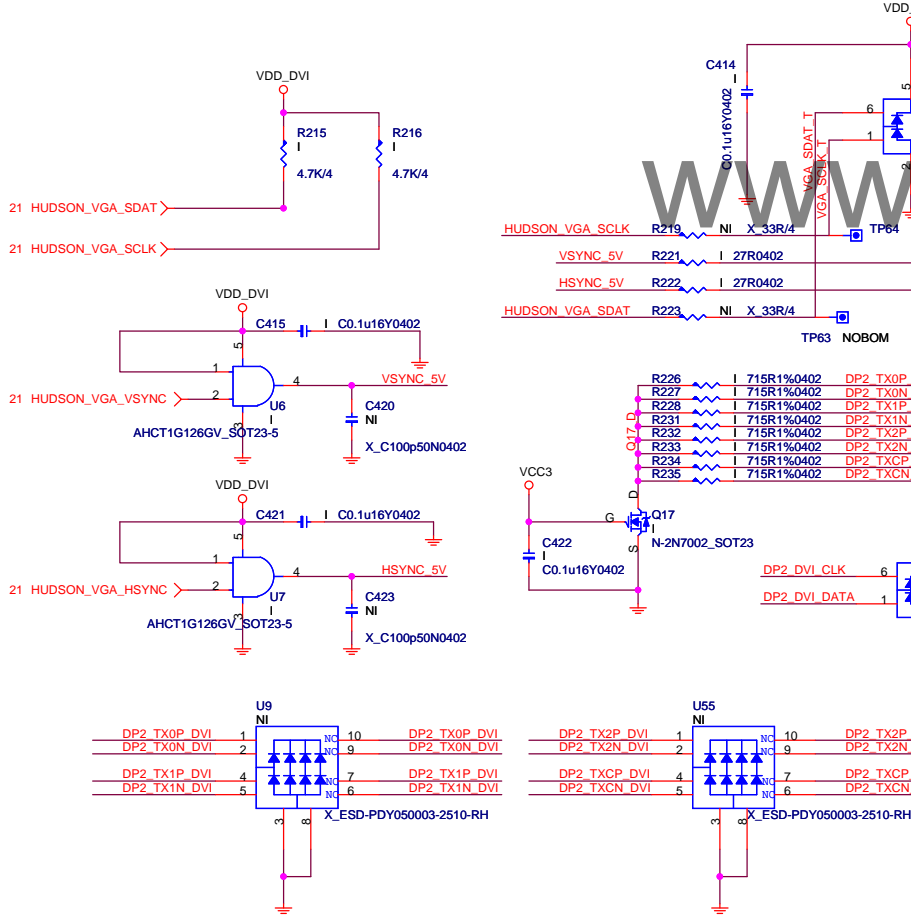
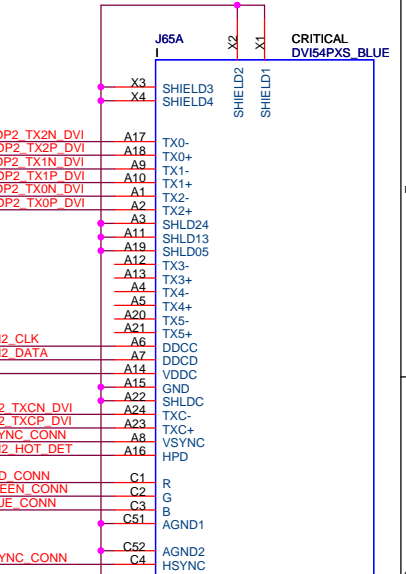
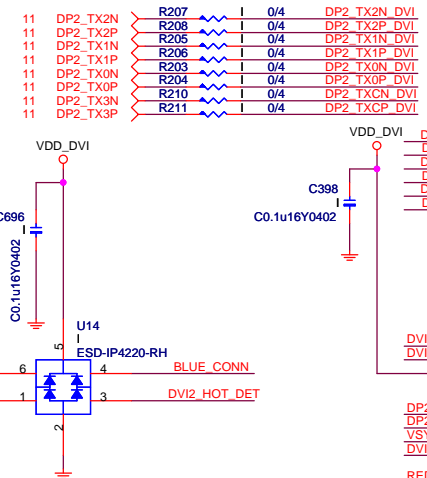
Size C	Document Description DVII CONN.	Re (
Date:	Sheet	24 of 45

DVI2 CONNECTOR

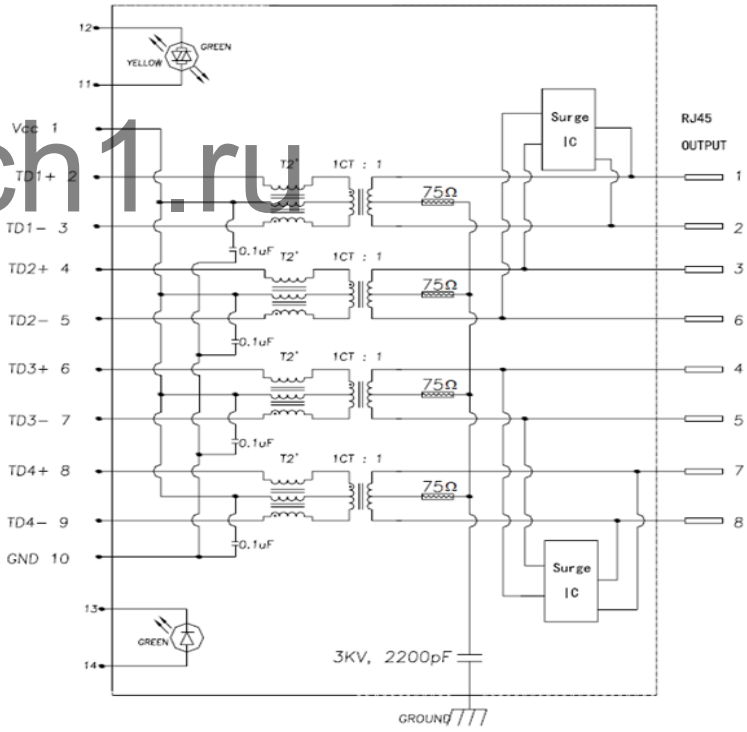
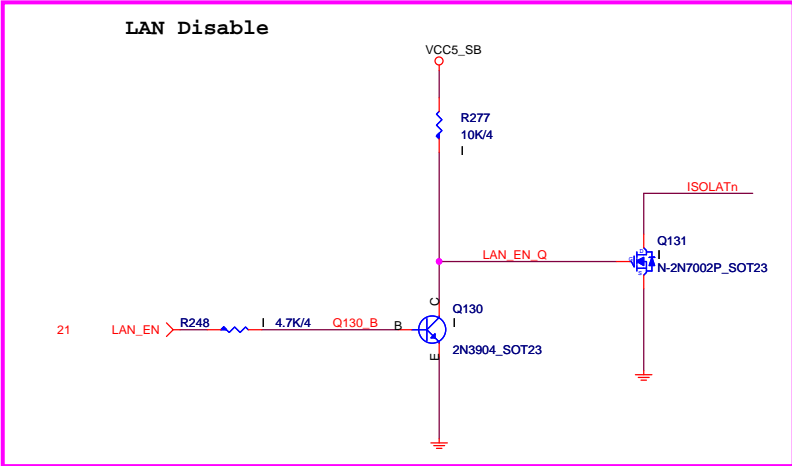
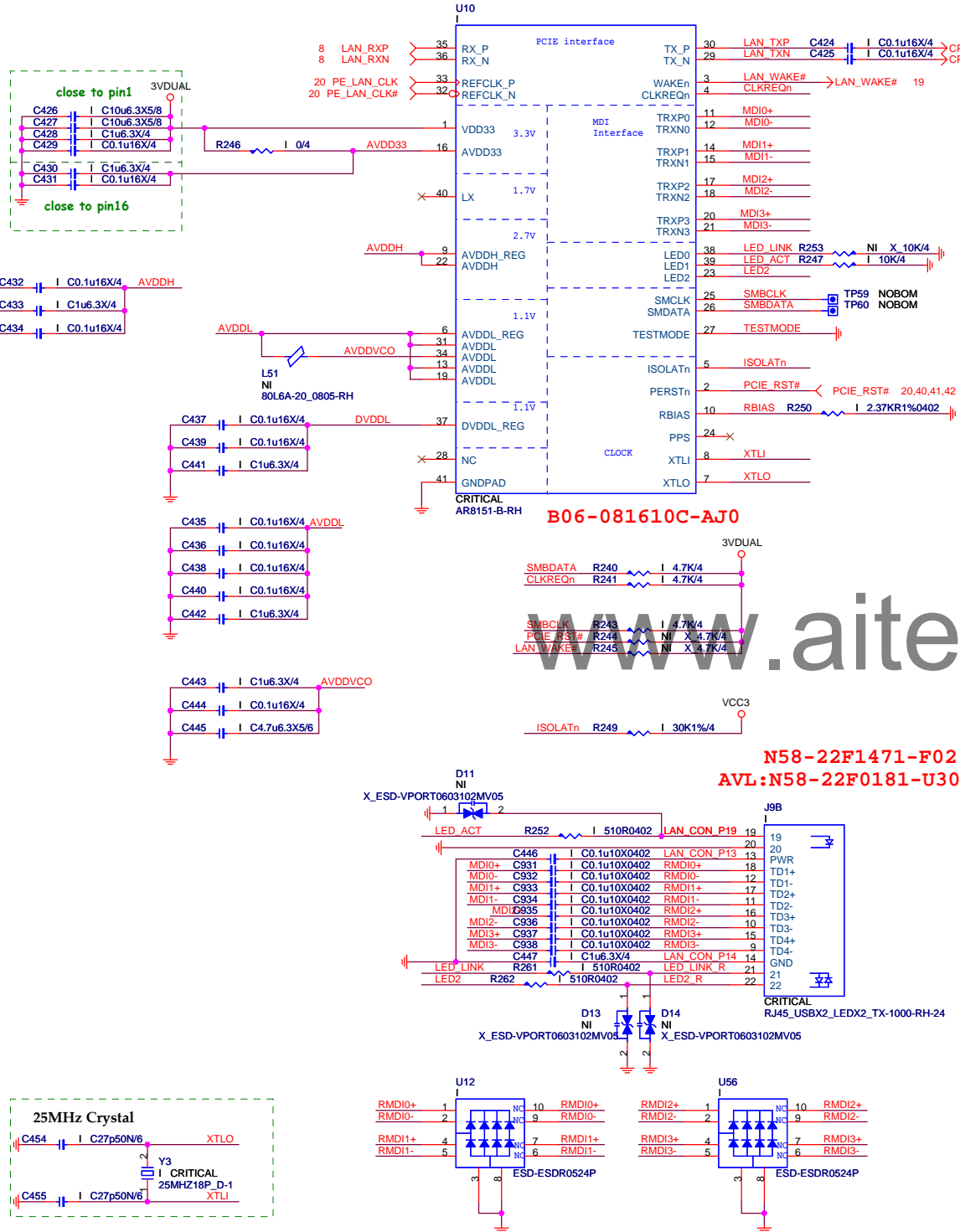
R932-R934 CLOSE TO CRT CONNECTOR, THE TRACE IMPEDANCE BETWEEN NB AND 150OHM
RESISTOR SHOULD BE 370HM+/-15%, THE
TRACE IMPEDANCE BETWEEN THE 2 150OHM
RESISTOR SHOULD BE 50 OHM +/-15%
THE IMPEDANCE BETWEEN THE 2ND RESISTOR
TO THE CONNECTOR SHOULD BE 750HM+/-15%



PLACE ESD PROTECTION DIODES
1. CLOSE TO CONNECTOR PINS
2. DIRECTLY ON SIGNAL TRACES
3. +5V & GND TRACE TO DIODE SHOULD BE
LESS THAN 100MILS AND 20MILS WIDE
4. THE ESD DIODE SHOULD BE THE FIRST DEVICE
FROM CONNECTOR



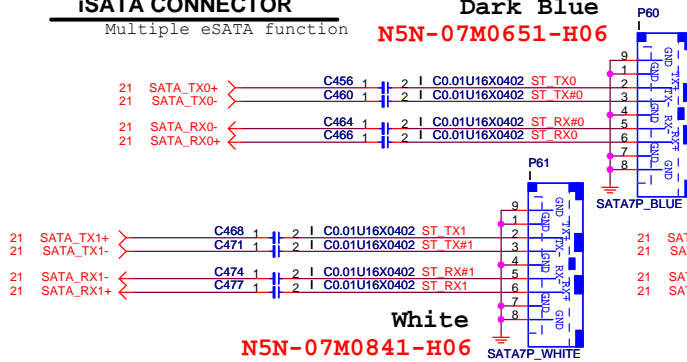
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HP SCH P/N: (MSI MS-7778)		
Size Custom	Document Description	Rev 0A
Date:	DVI2 CONN.	Sheet 25 of 45



iSATA CONNECTOR

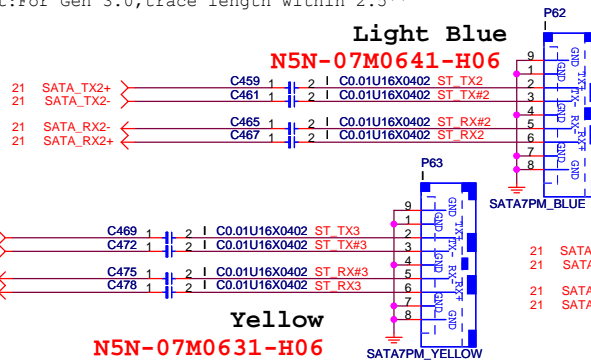
Multiple eSATA function

Dark Blue
N5N-07M0651-H06

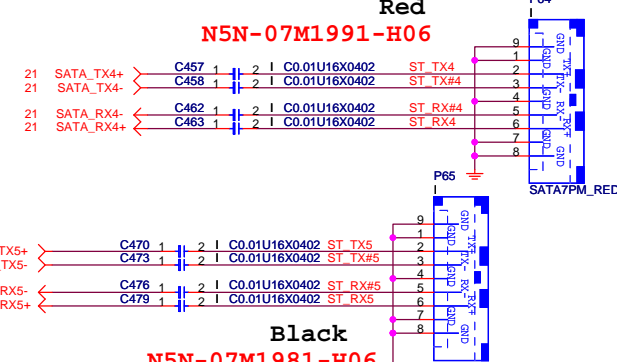


Layout:For Gen 3.0,trace length within 2.5''

Light Blue
N5N-07M0641-H06



Red
N5N-07M1991-H06



White
N5N-07M0841-H06

Yellow
N5N-07M0631-H06

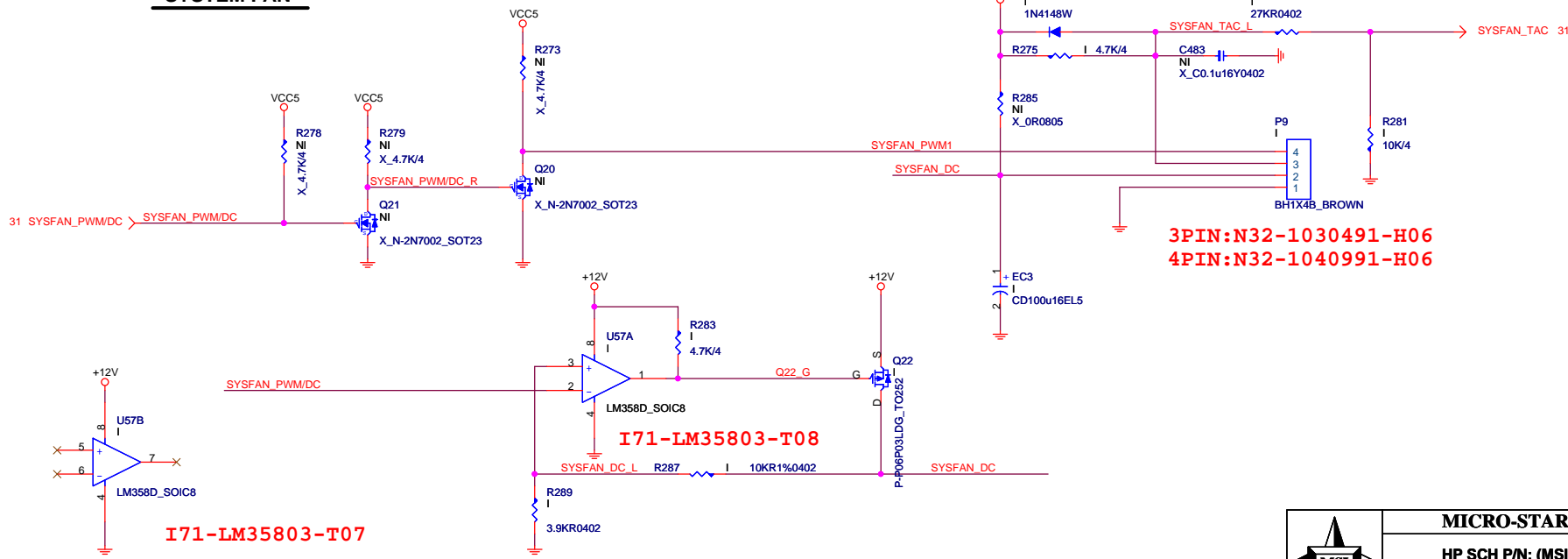
Black
N5N-07M1981-H06

PWM FAN CONTROL

CPU FAN



SYSTEM FAN



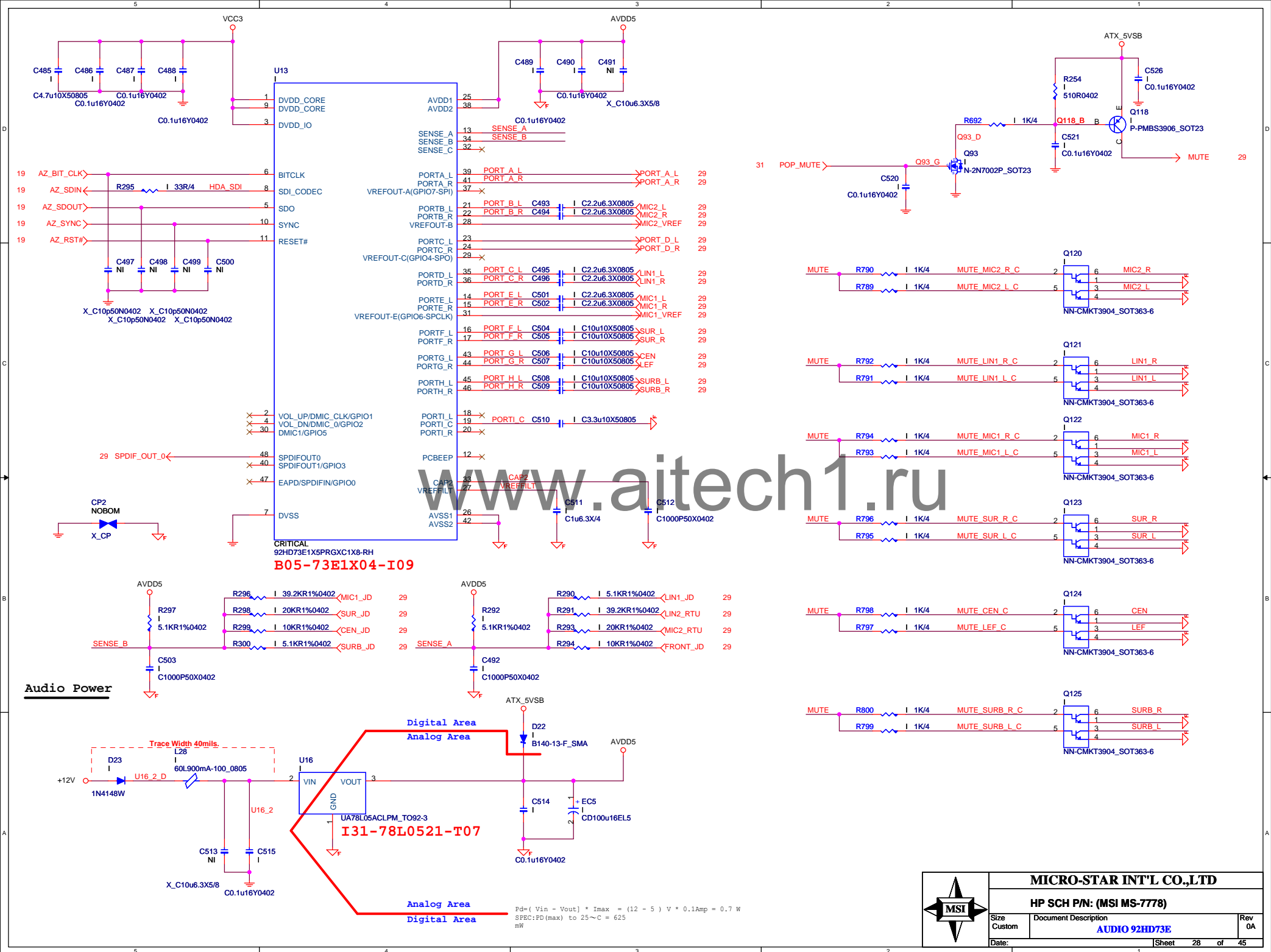
3PIN:N32-1030491-H06
4PIN:N32-1040991-H06

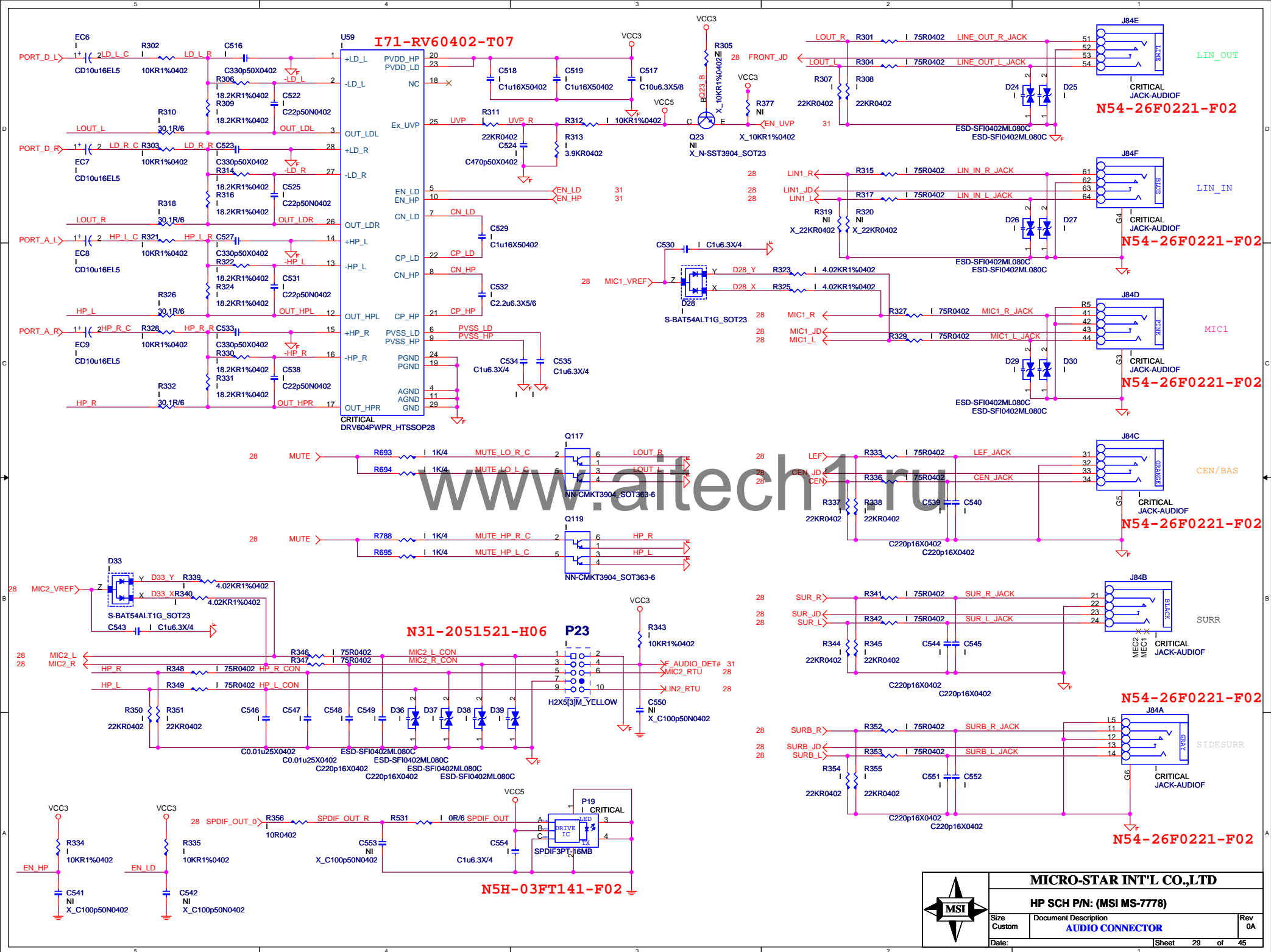


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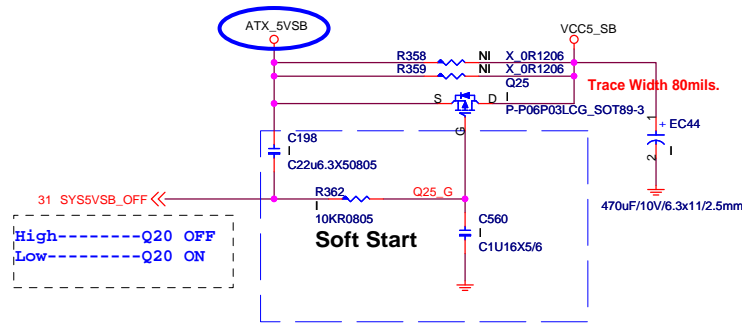
HP SCH P/N: (MSI MS-7778)

Size	Document Description	Rev
Custom	SATA/FAN	0A
Date:	Sheet 27 of 45	

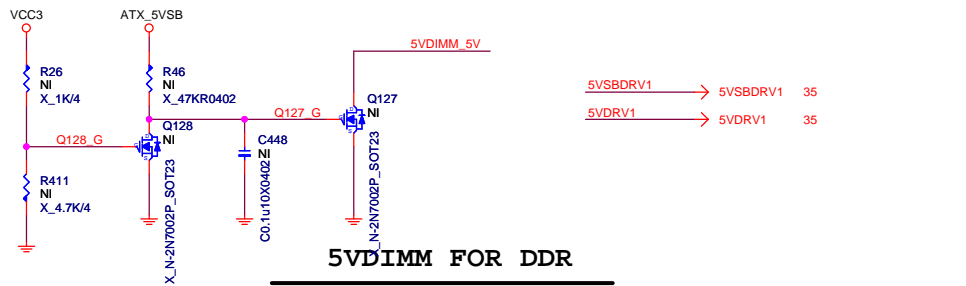




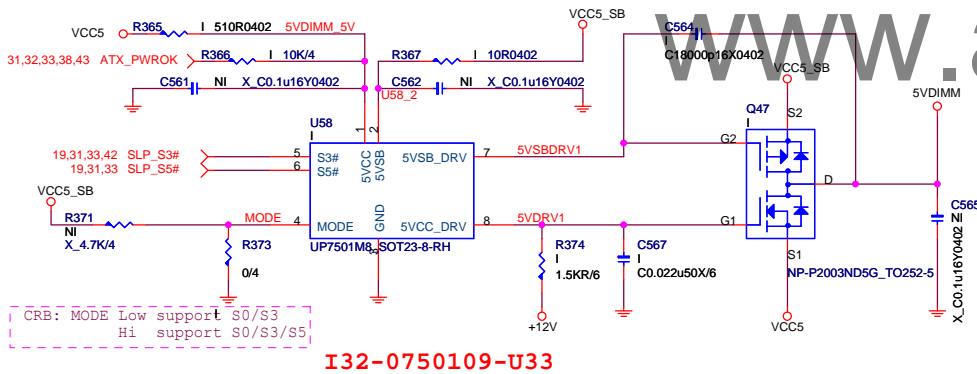
VCC5 SB Power Switch



For special PSU sequence

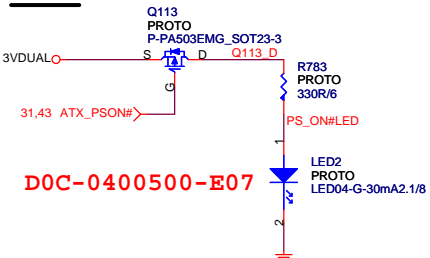


5VDRV1 FOR DDR



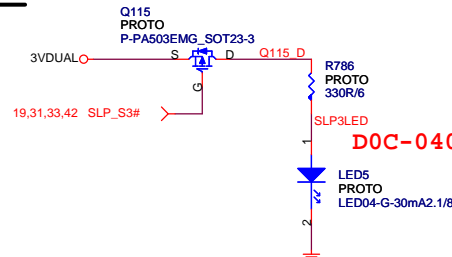
I32-0750109-U33

PS_ON#



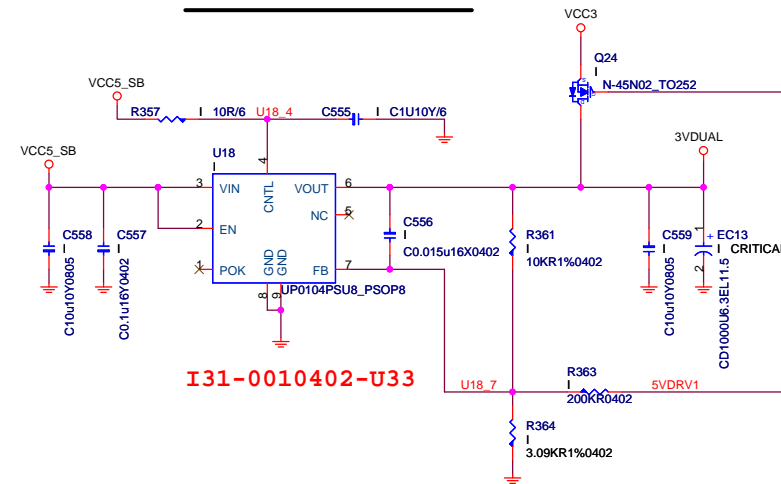
D0C-0400500-E07

SLP_S3#



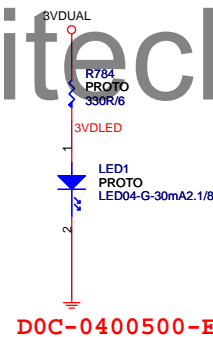
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3VDUAL POWER



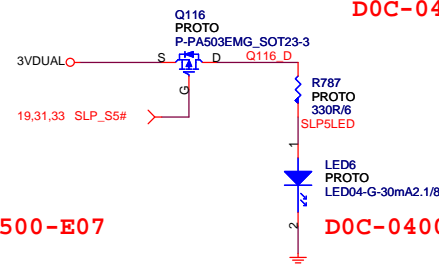
I31-0010402-U33

3VDUAL



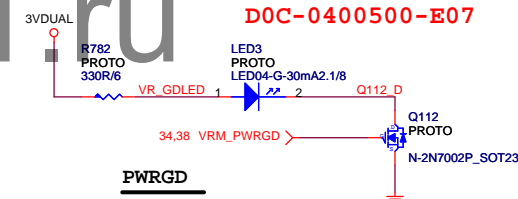
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SLP_S5#



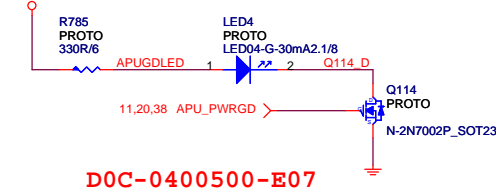
D0C-0400500-E07

VRMPWRGD



D0C-0400500-E07

PWRGD



D0C-0400500-E07



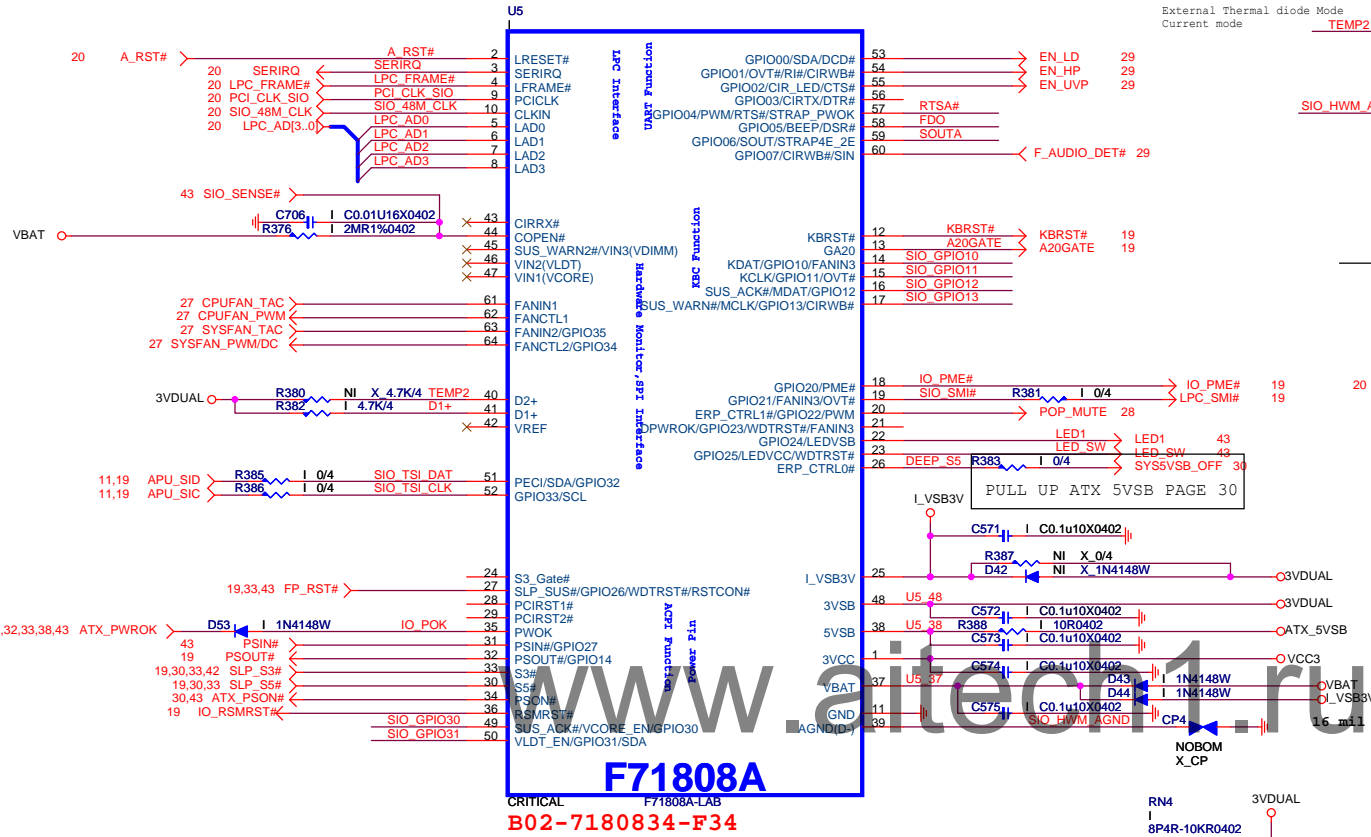
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: (MSI MS-7778)

Size	Document Description	Rev
Custom	ACPI UPI & LED	0A
Date:	Sheet 30 of 45	

F71808A

TEMP SENSOR



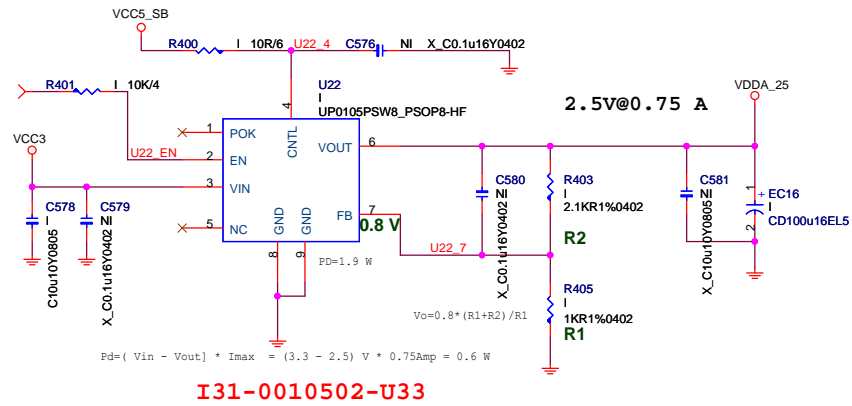
PIN	Function	NET Name	HI	LO
64	FANCTRL2	FANCTRL2	PWM FAN	LINEAR FAN
59	STRAP4E_2E	SOUTA	4E (DEFAULT)	2E
57	STRAP_PWOK	RTSA#	AMD (DEFAULT)	INTEL



MICRO-STAR INT'L CO.,LTD			
HP SCH P/N: (MSI MS-7778)			
Size Custom	Document Description	SUPER I/O F71808A	
Date:	Sheet 31	of	45

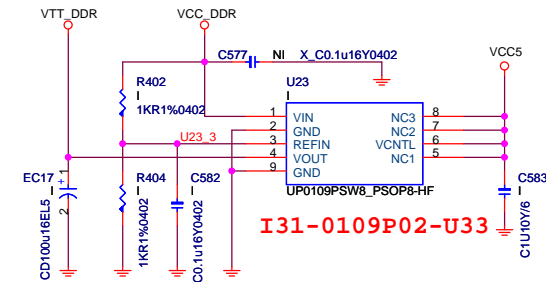
CPU VDDA_25 POWER

Layout:Route 50 mils AND 500 mils LONG
(USE 2x25 mil TRACES TO EXIT BALL FIELD)



VTT_DDR POWER

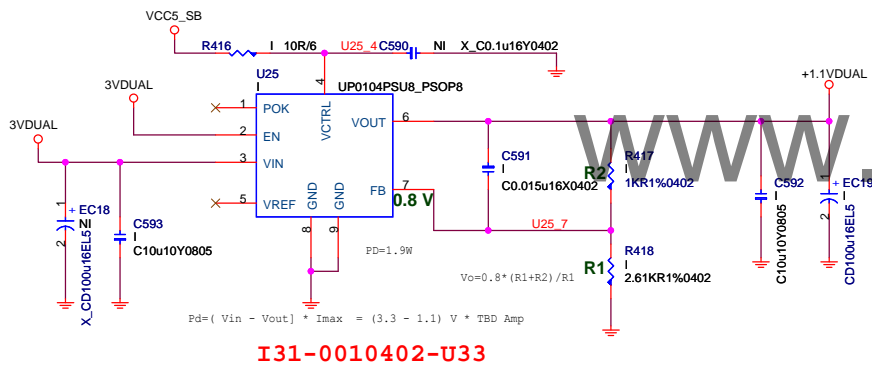
0.75V@2A



1.1VDUAL POWER

1.V@1.3A----D3

S0,S1,S3



MICRO-STAR INT'L CO.,LTD

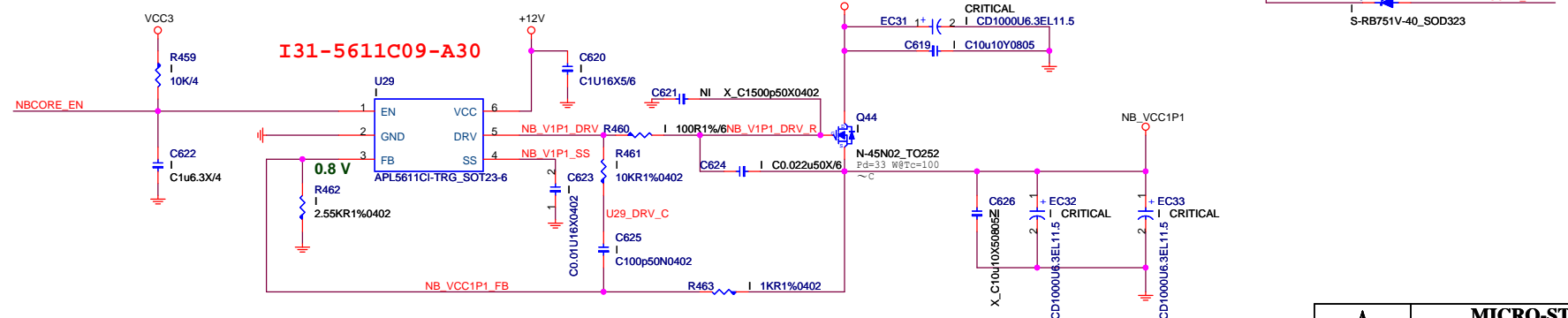
HP SCH P/N: (MSI MS-7778)

Size Custom	Document Description SYS POWER	Rev 0A
Date:	Sheet 32 of 45	

1.2V@15A



1.1V@5A



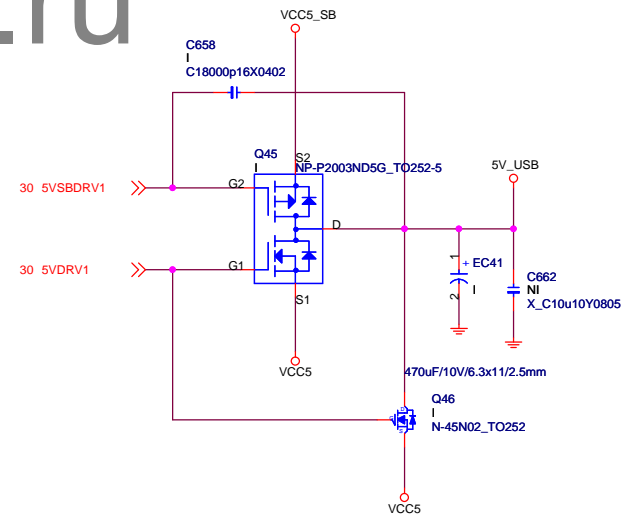
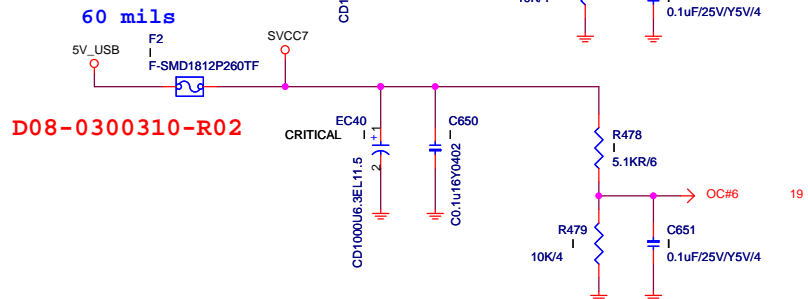
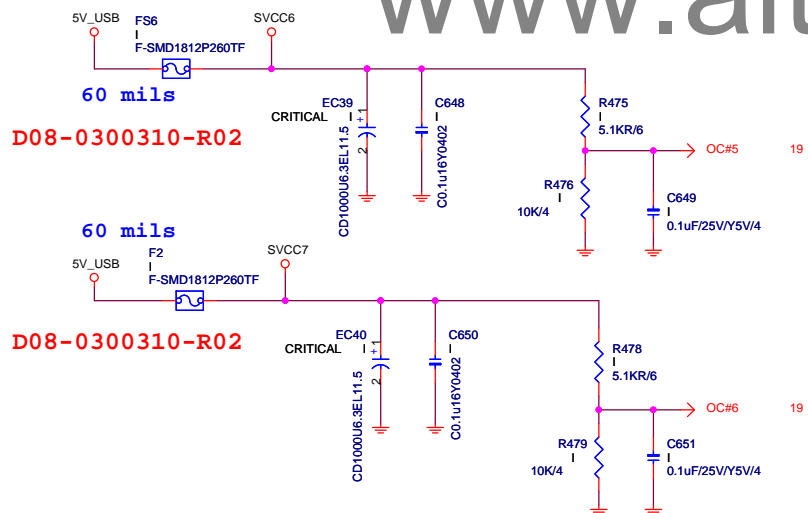
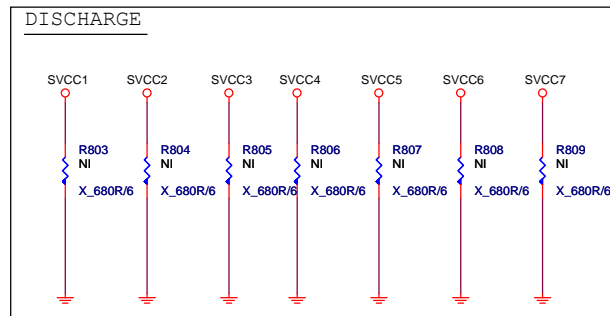
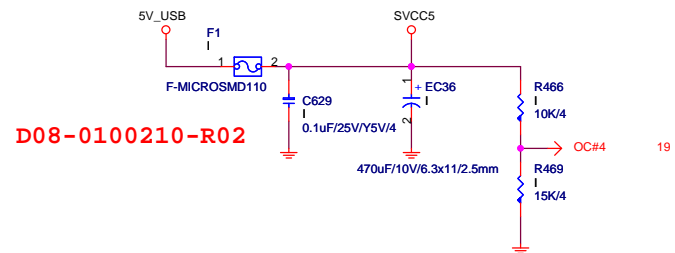
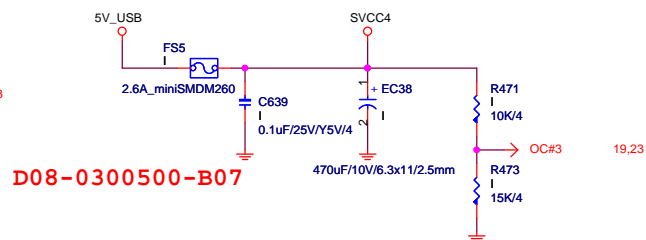
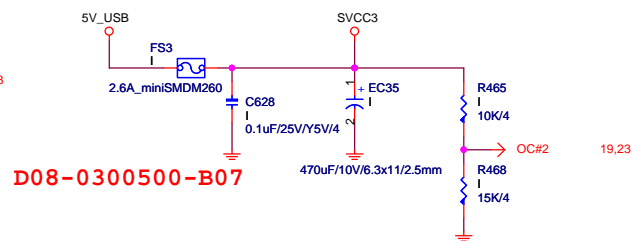
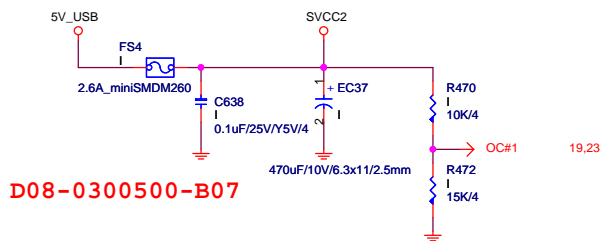
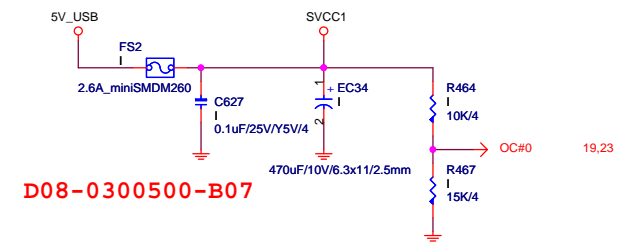
HP SCH P/N: (MSI MS-7778)

Size	Document Description
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Rev	0A
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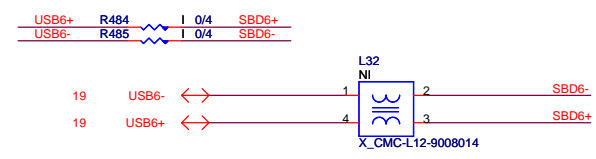
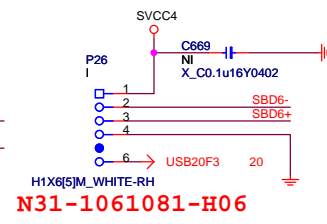
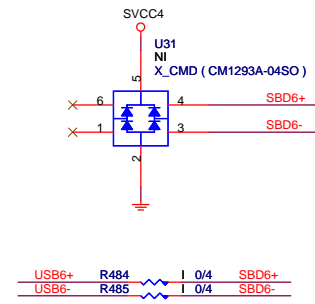
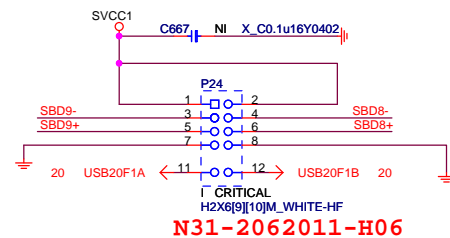
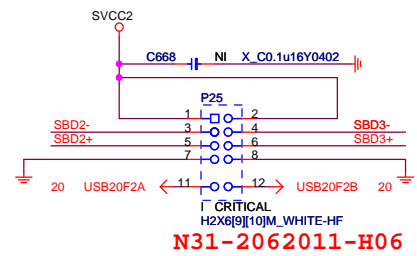
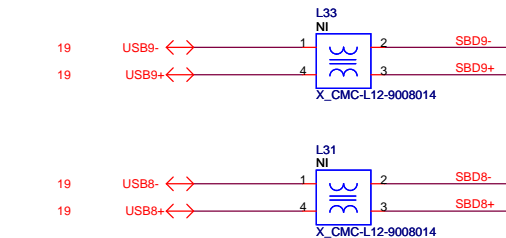
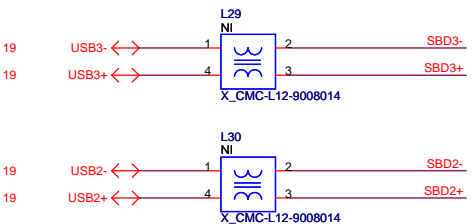
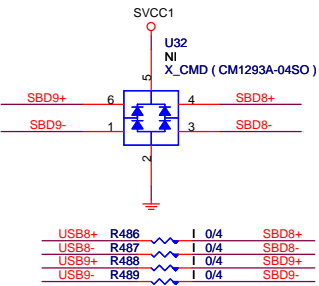
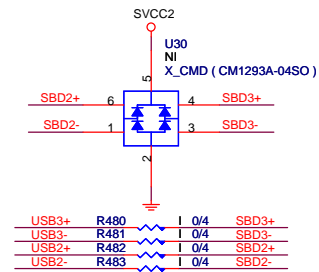
Date:	Sheet 34 of 45
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USB POWER



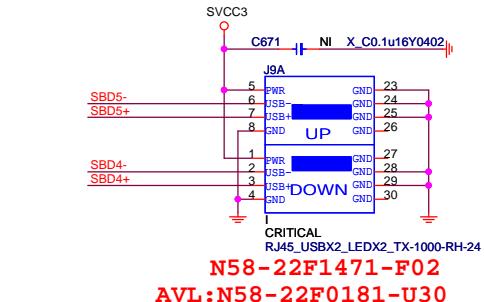
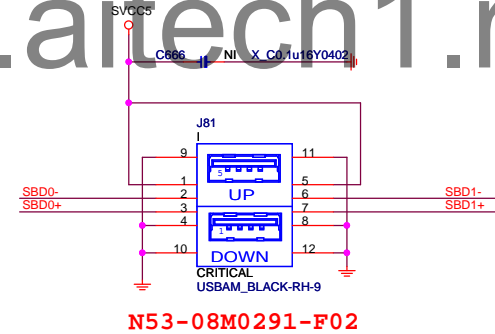
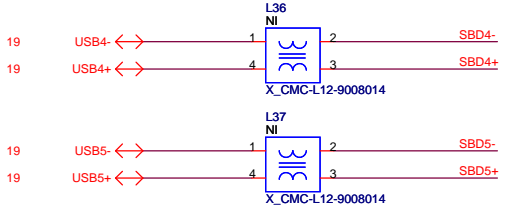
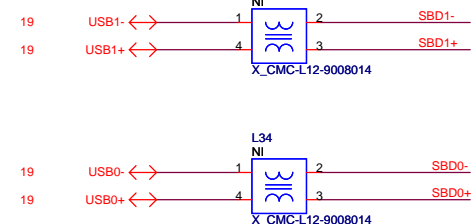
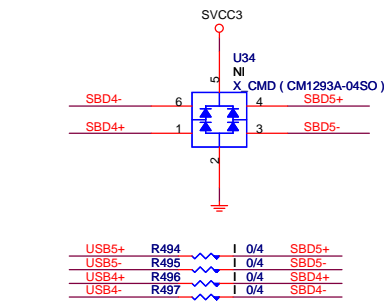
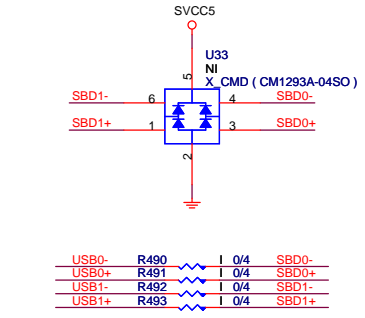
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FRONT USB PIN HEADER




USB 2.0 trace length
FRONT side within 6'';
REAR side within 18''

REAR PANEL USB 2.0 CONNECTOR

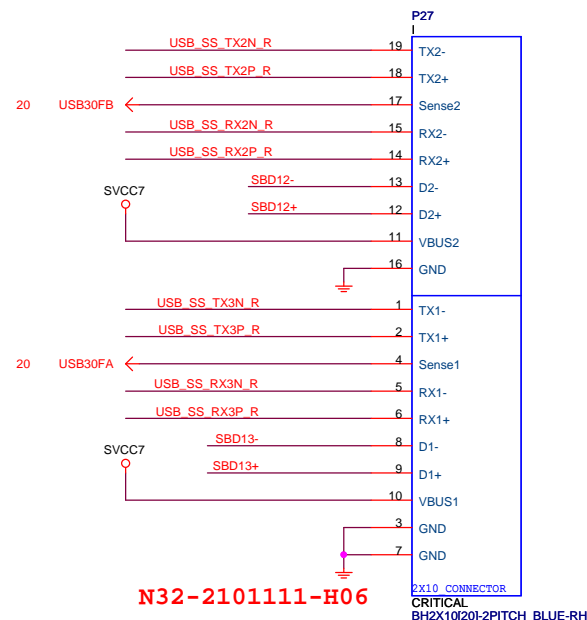
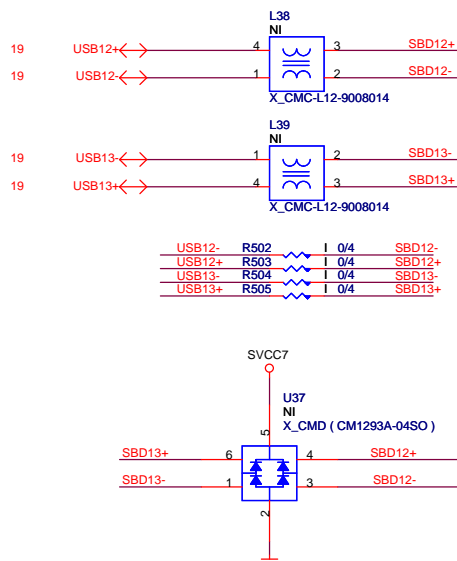
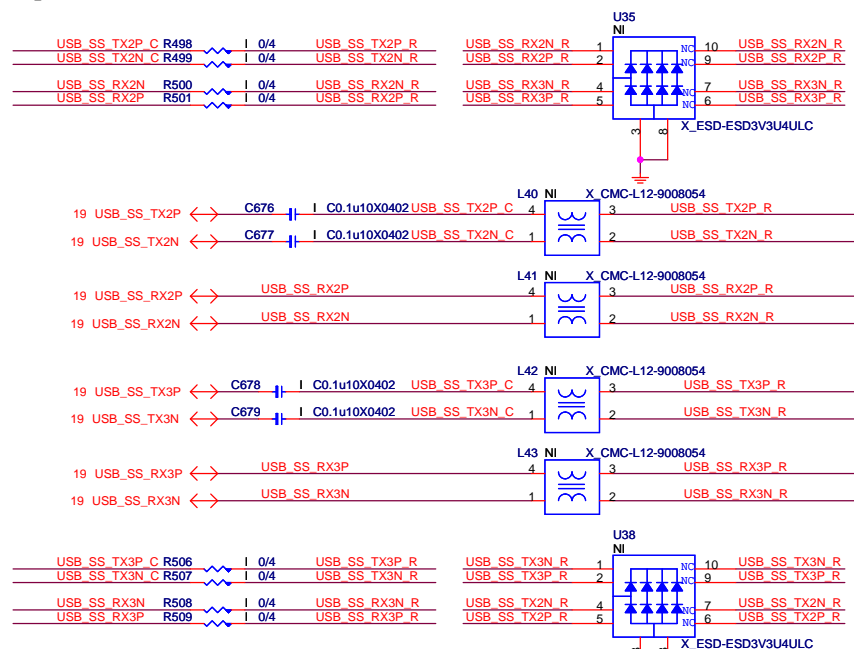


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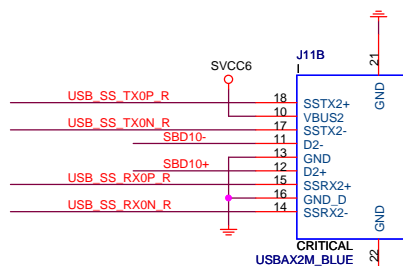
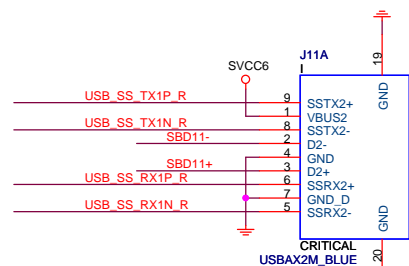
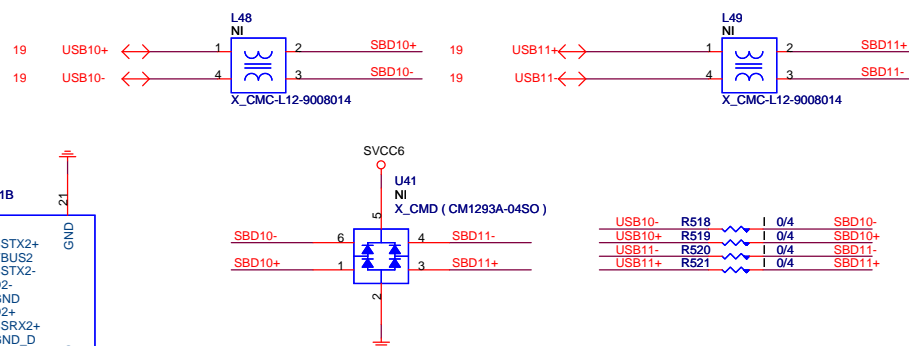
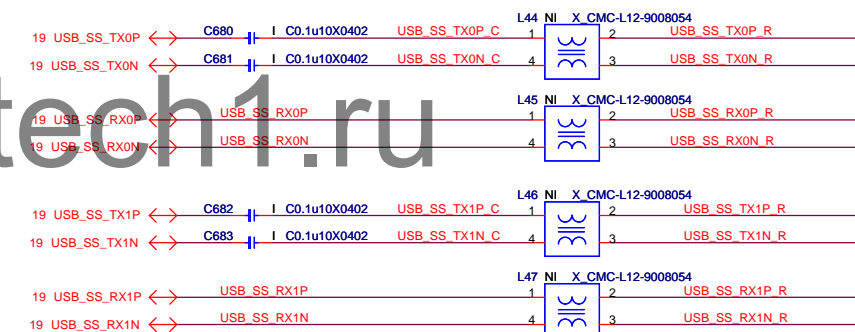
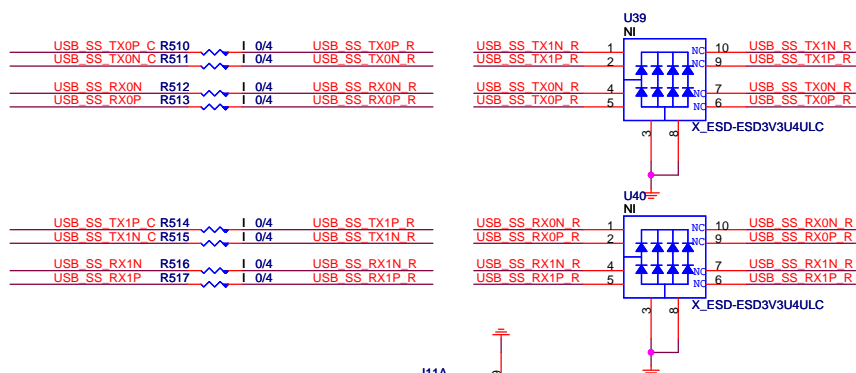
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Size Custom	Document Description	Rev 0A
USB 2.0 CONN		
Date:	Sheet 36	of 45

E	
USB 3.0 trace length	
Front pin header within 3.5"	



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USB 3.0 trace length
Rear connector within 8"



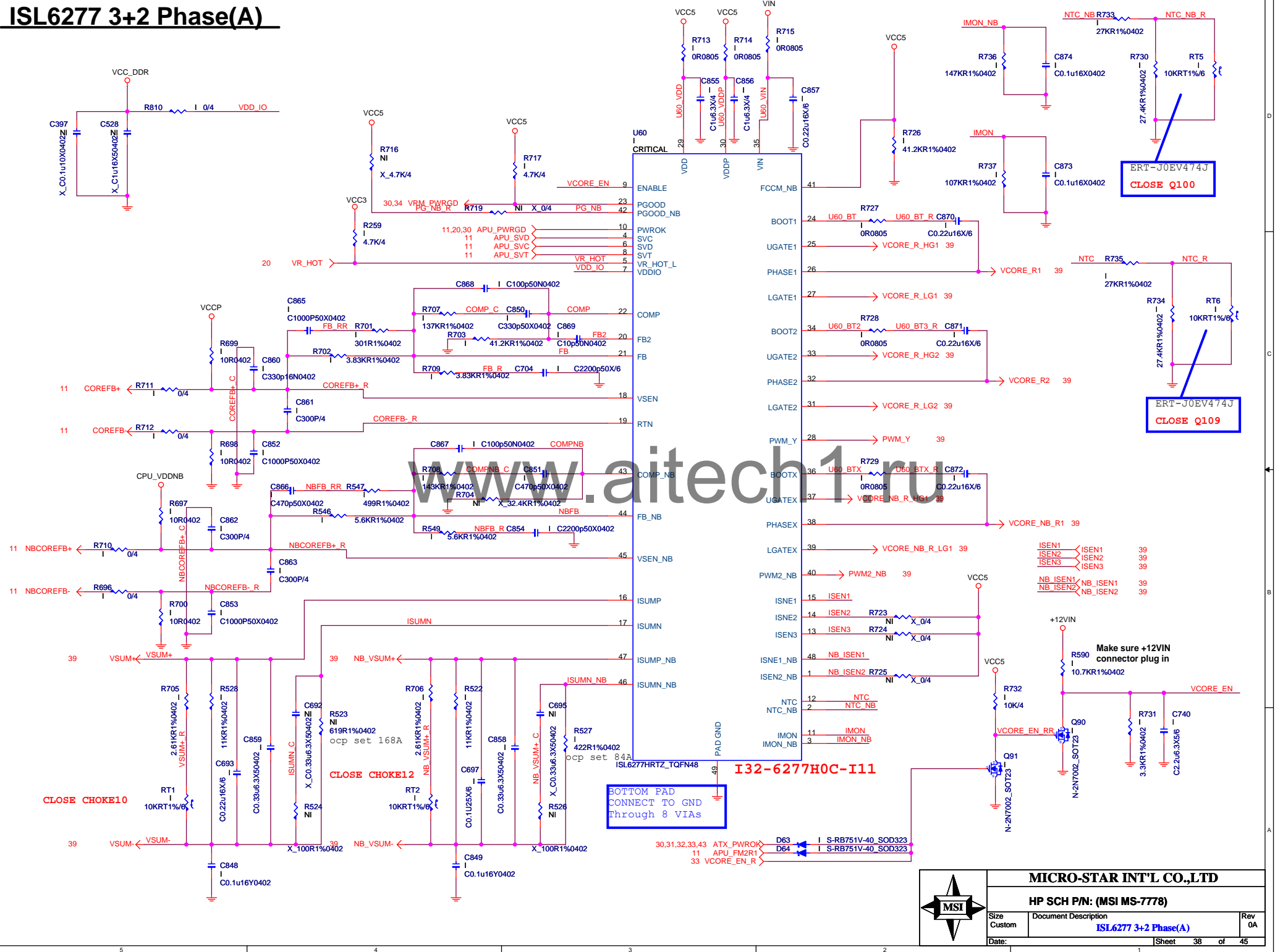
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Rev
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ISL6277 3+2 Phase(A)

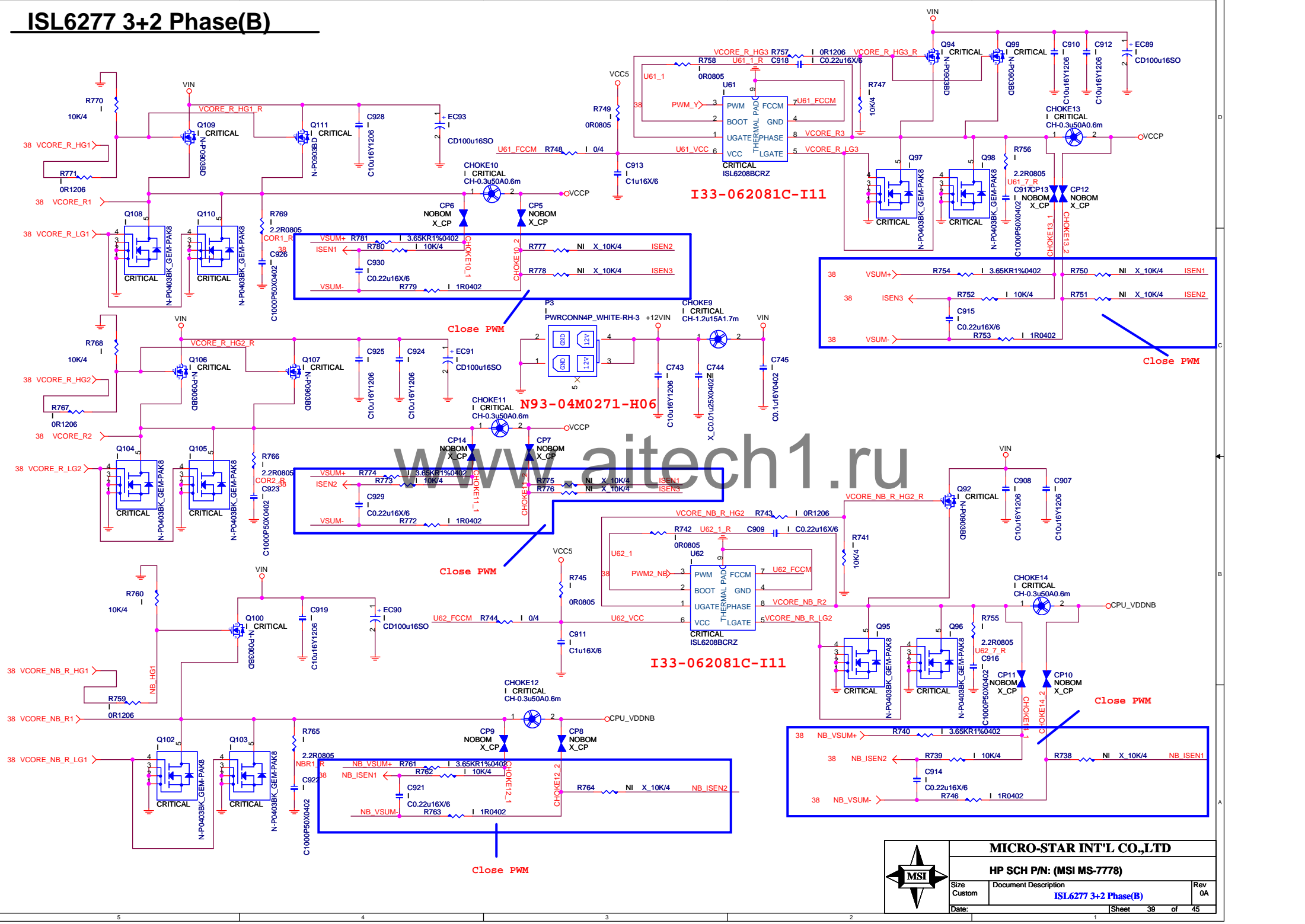


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Size Custom	Document Description ISL6277 3+2 Phase(A)	Rev 0A
Date:	Sheet 38 of 45	

ISL6277 3+2 Phase(B)



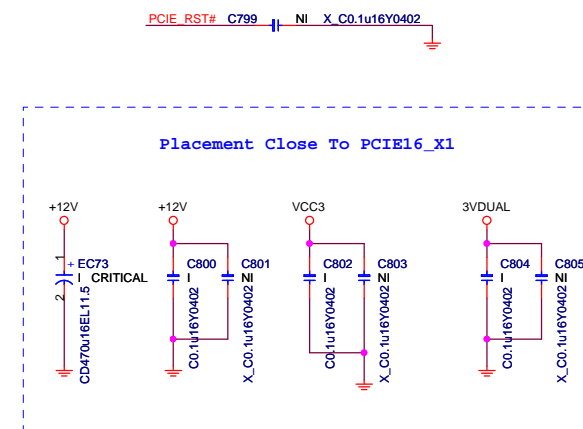
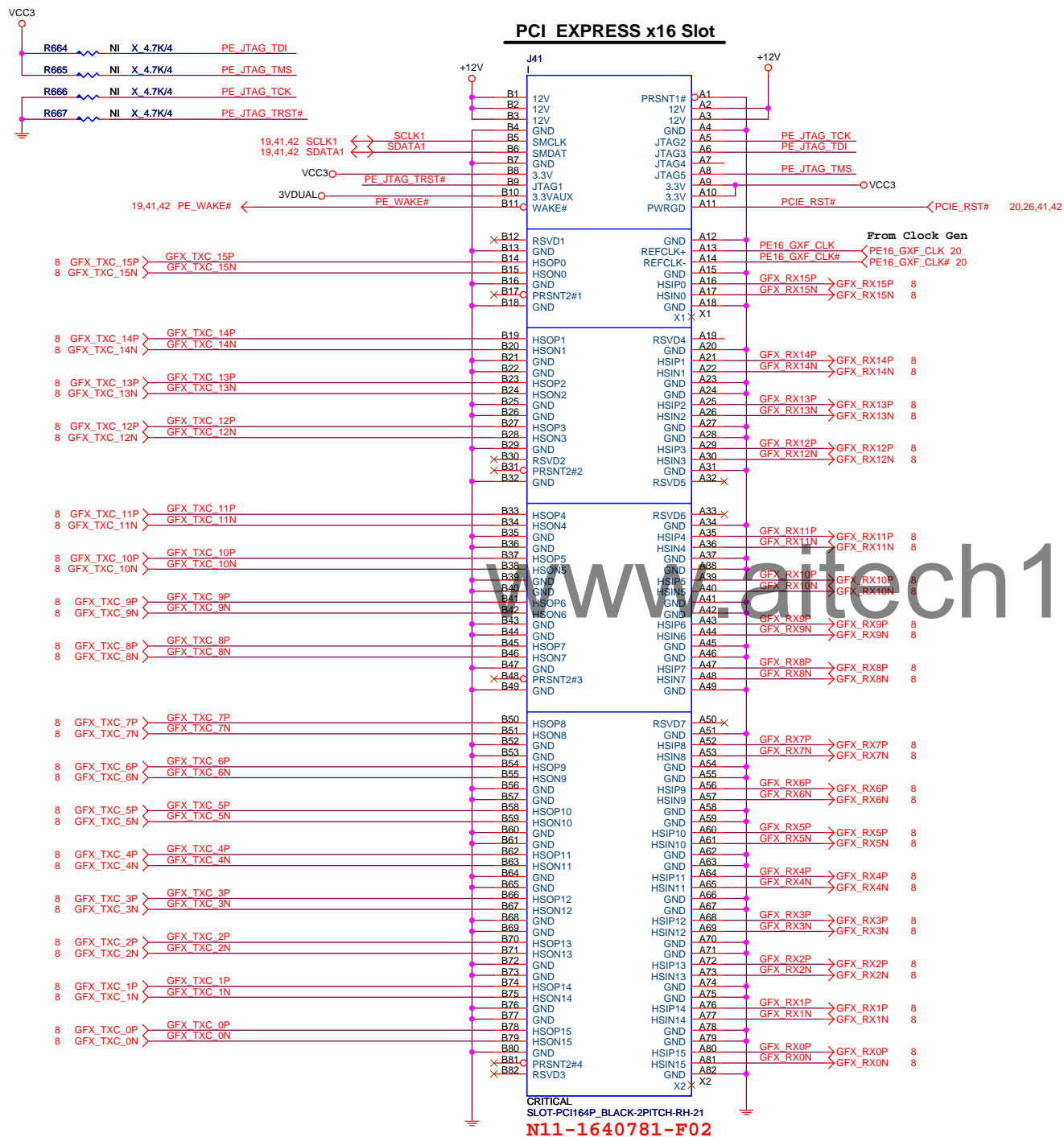
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Date:
Sheet 39 of 45

PCI Express Slot x16



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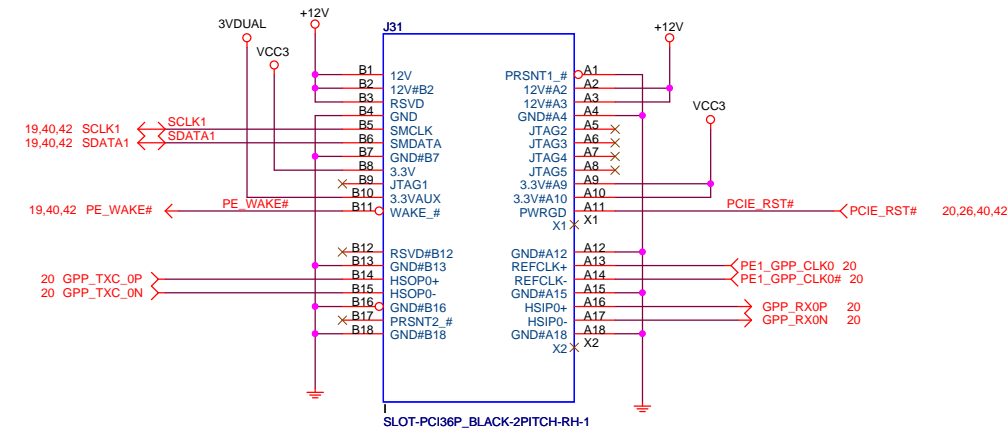
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PCIE X16 SLOT

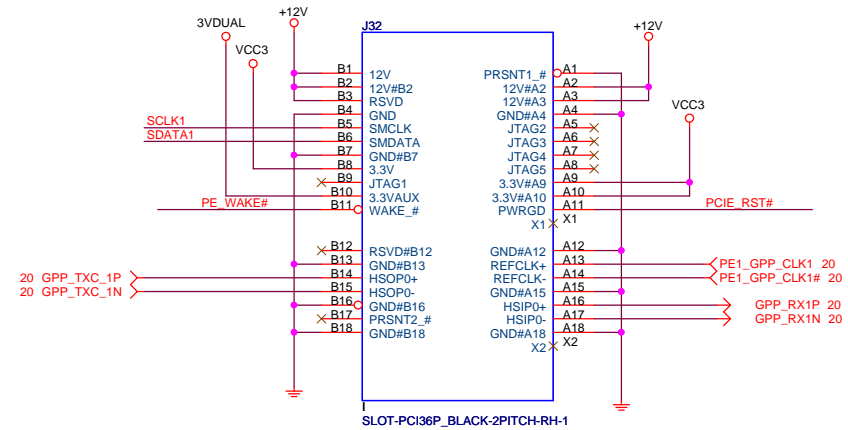
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PCI EXPRESS X1 Slot-1



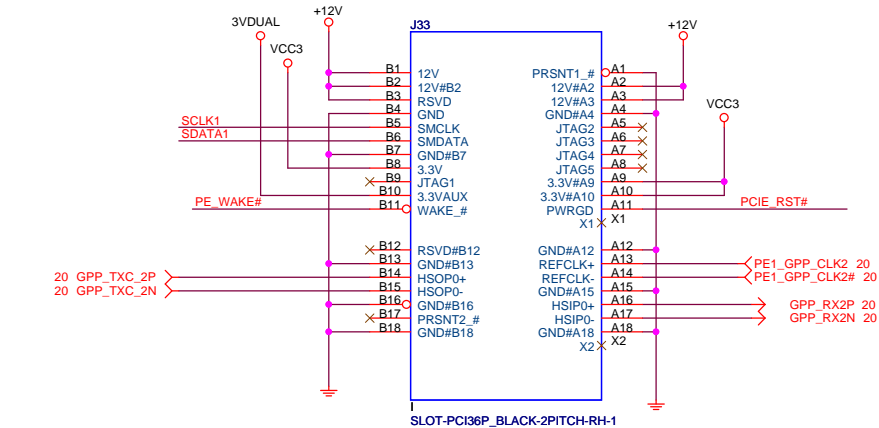
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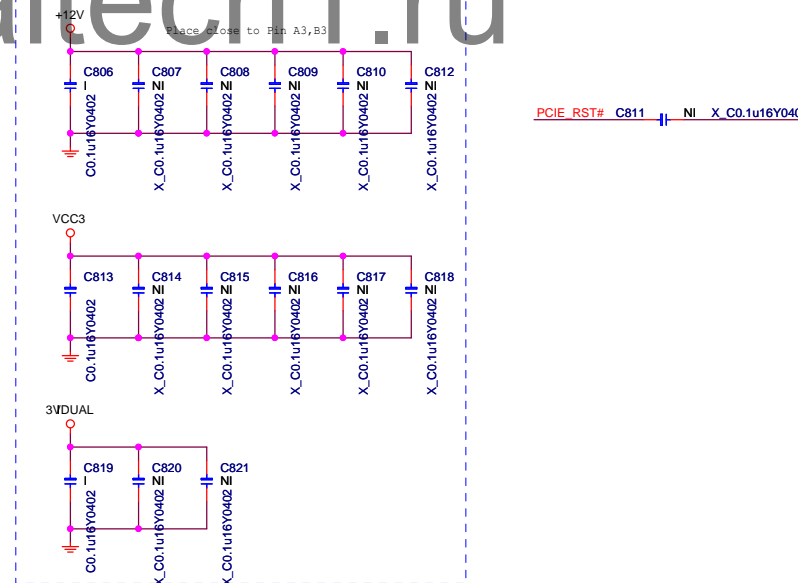
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PCI EXPRESS X1 Slot-3



N11-0360251-F02

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Size
Custom

Document Description

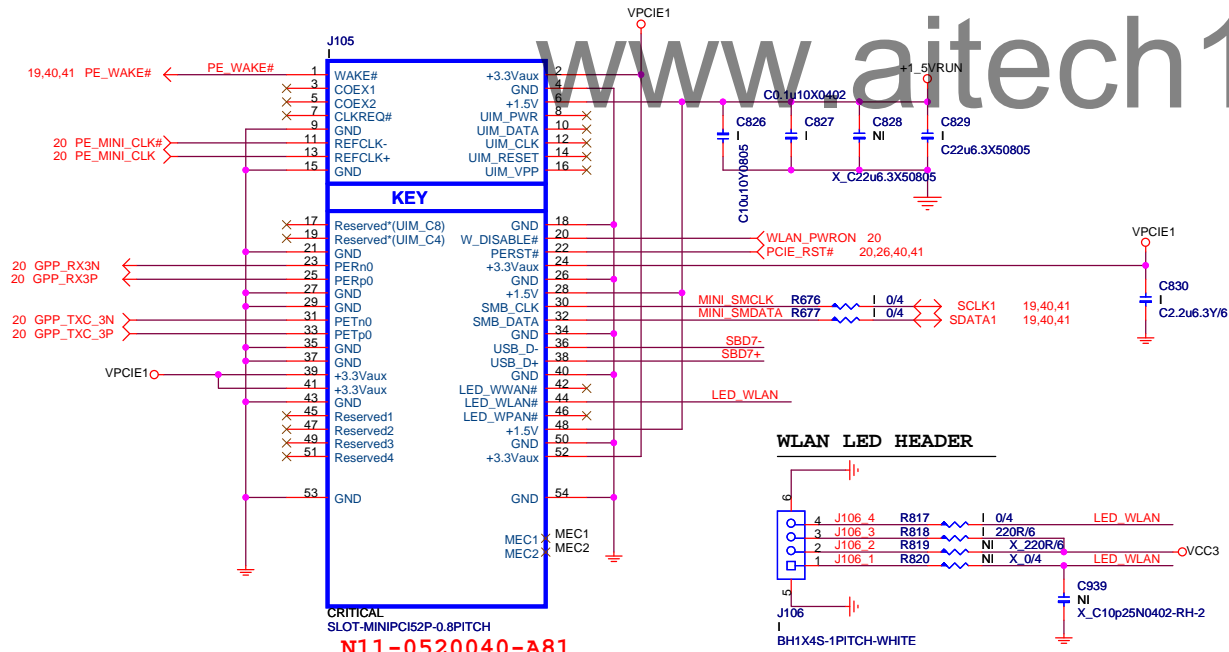
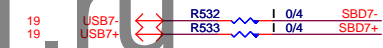
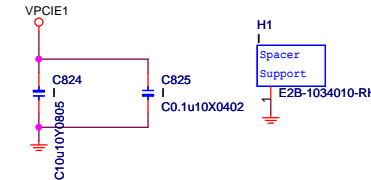
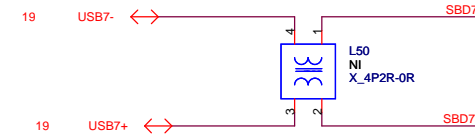
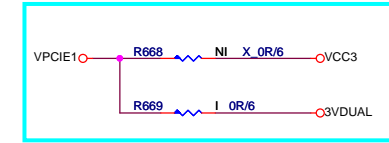
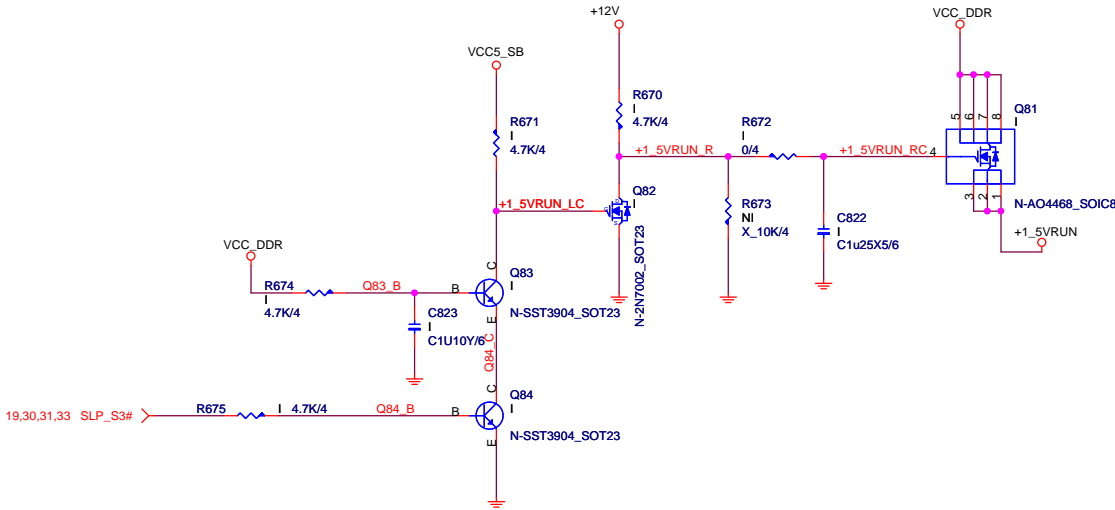
PCI E X1 SLOTS

Rev
0A

Date:

Sheet 41 of 45

Wireless LAN(Short Card)



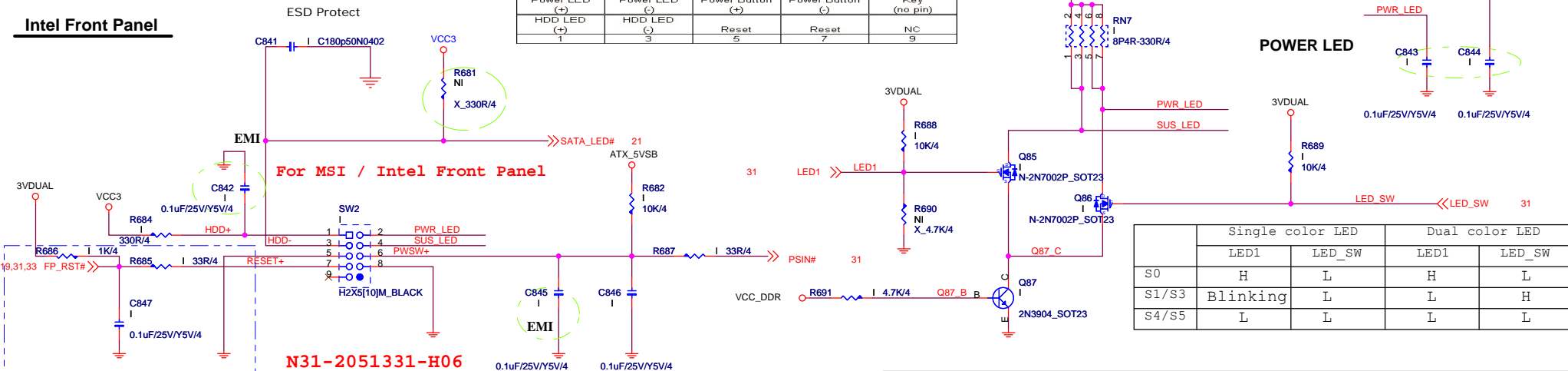
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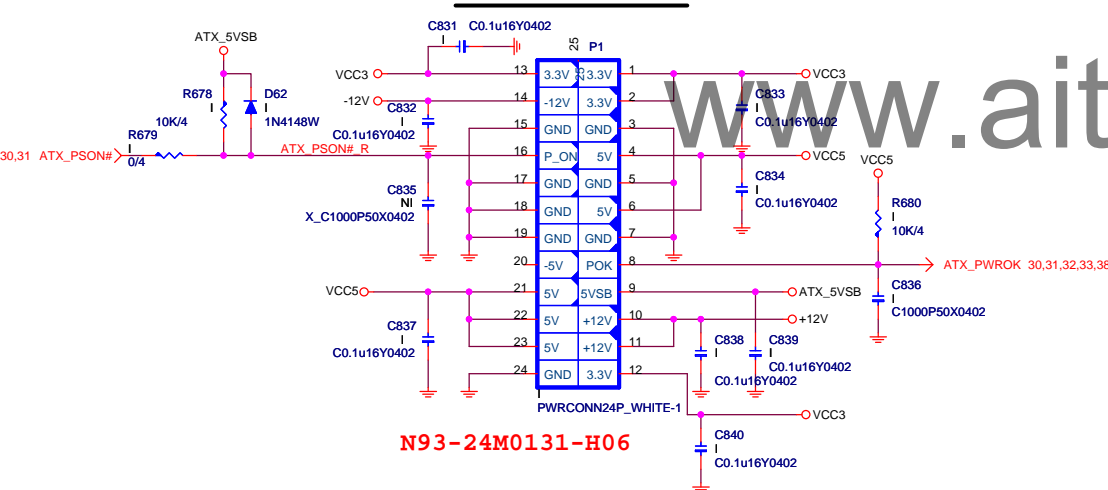
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Date:	PCIE X1 mini card	

ATX connector / Front Panel

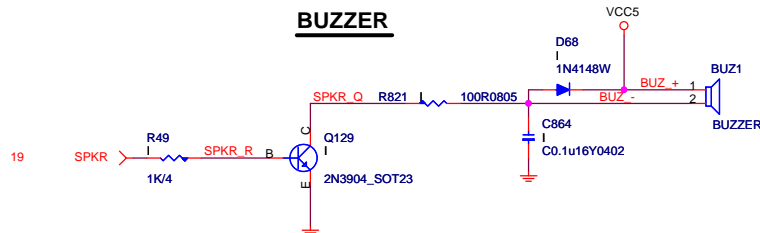
Intel Front Panel



ATX CONNECTOR



BUZZER

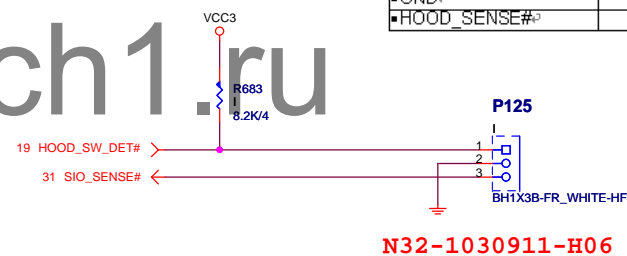


HP Restricted Secret

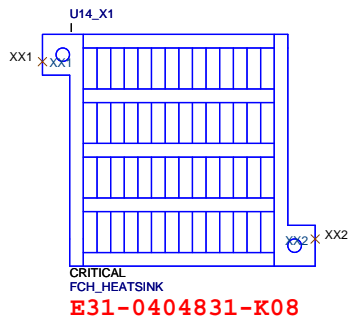
HOOD SENSE

P125 - HOOD SENSE HEADER PIN DESCRIPTION

SIGNAL NAME	PIN #
HOOD SW DET#	1
GND	2
HOOD SENSE#	3

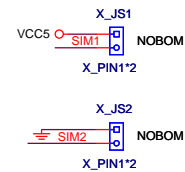


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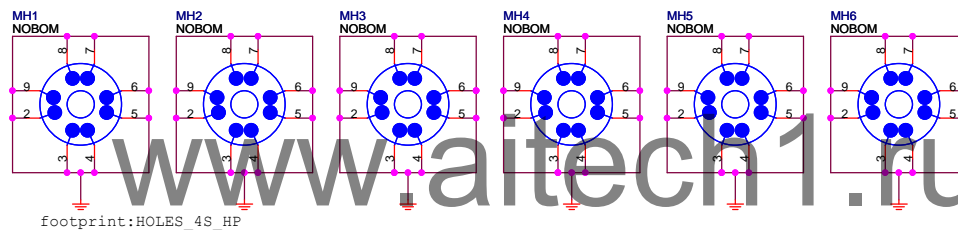


MANUAL PART

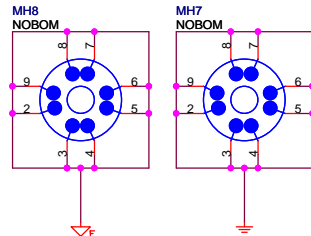
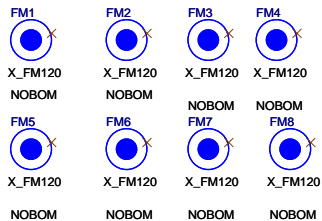
Simulation



Mounting Holes



Optics Orientation Holes




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Size Custom	Document Description Auto BOM manual	Rev 0A
Date:	Sheet 1	44 of 45

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Size Custom	Document Description History		Rev 0A
Date:	Sheet 45 of 45		1